



# PEER REVIEWERS

*This book has been technically reviewed by the following experts in the PCB industry.*

## Eric Bogatin



Eric Bogatin is currently the dean of the Teledyne LeCroy Signal Integrity Academy. Additionally, he is an adjunct professor at the University of Colorado-Boulder in the ECEE department, where he teaches a graduate class in signal integrity and is also the editor of *Signal Integrity Journal*. Bogatin received his BS in physics from MIT, and MS and PhD in physics from the University of Arizona in Tucson. He has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansoft and Interconnect Devices. Bogatin has written six technical books in the field, and presented classes and lectures on signal integrity worldwide.

## Rick Hartley



Rick Hartley is the principal of RHartley Enterprises, through which he consults and teaches internationally to resolve noise, signal integrity and EMI problems. Hartley's focus is on the correct design of PC boards to prevent and solve problems. His design career has focused on circuits and PC boards for computers, aircraft avionics and telecommunications. His consulting efforts have also focused on the automotive and appliance spaces. Hartley has a degree in engineering from Ohio Technical Institute and 51 years of experience. He has dedicated the past 40 years to PC board and circuit development with emphasis on control of noise, in digital, analog and RF circuits. Rick is a member of the IPC Designers Council executive board, and past national chairman of the Designers Council. Rick has written numerous technical papers and articles on methods to control noise, EMI and signal integrity.

# MEET THE AUTHOR

## Martyn Gaudion

Managing Director of Polar Instruments



Martyn Gaudion began his career in the early 1980s at Tektronix, where he was responsible for test engineering on high-bandwidth portable oscilloscopes. During his time at Tektronix, he gained widespread experience in PCB assembly and was extensively involved with the introduction of surface mount technology.

In 1990, Gaudion joined Polar, where he was responsible for the design and development of the Toneohm 950, Polar's multilayer PCB short circuit locator. He became marketing manager at Polar during 1997 as the market for controlled impedance test became a major section of Polar's product range. He was appointed sales and marketing director in 2001 and CEO in 2010. Gaudion also writes occasional articles for a number of PCB industry publications, and regularly contributes to IPC's High-Speed High-Frequency standards development activities.

Gaudion is a chartered company director and a fellow of the London-based IoD (Institute of Directors). In 2016, he was appointed vice chairman of the European Institute of Printed Circuits (EIPC).

# The Printed Circuit Designer's Guide to...™ Secrets of High-Speed PCBs

PART 1

*Specifying, Modelling, and Measuring*

**Martyn Gaudion**

Polar Instruments

© 2017 BR Publishing, Inc.  
All rights reserved.

BR Publishing, Inc.  
dba: I-Connect007  
PO Box 50  
Seaside, OR 97138-0050

ISBN: 978-0-9796189-6-3

**I-Connect007**  
GOOD FOR THE INDUSTRY

Visit [I-007eBooks.com](http://I-007eBooks.com) for more books in this series.



# The Printed Circuit Designer's Guide to...™

## Secrets of High-Speed PCBs, Part 1

### Contents

PAGE

<b>1</b>	<b>Introduction</b>
<b>5</b>	<b>Chapter 1</b> <i>Material Matters or Materials Matter?</i>
<b>13</b>	<b>Chapter 2</b> <i>Correlation, Communication, Calibration</i>
<b>19</b>	<b>Chapter 3</b> <i>Zen and the Art of Accurate Impedance Measurement</i>
<b>25</b>	<b>Chapter 4</b> <i>Transmission Lines: A Voyage from DC—no, not Washington, Part 1</i>
<b>31</b>	<b>Chapter 5</b> <i>Transmission Lines: A Voyage from DC—no, not Washington, Part 2</i>
<b>39</b>	<b>Chapter 6</b> <i>When is a 10GHz Transmission Line not a 10GHz Transmission Line?</i>
<b>45</b>	<b>Chapter 7</b> <i>Regional Differences: A Voyage of Glass Reinforcement</i>
<b>51</b>	<b>Chapter 8</b> <i>Crosshatching Compromise</i>
<b>55</b>	<b>Chapter 9</b> <i>Tolerant of Tolerance?</i>
<b>60</b>	<b>Summary</b>
<b>61</b>	<b>About Polar Instruments</b>



# INTRODUCTION

This is a guide for those involved in the procurement, design, or fabrication of high-speed impedance or insertion loss controlled PCBs.

Who should read this book? Certainly, PCB technologists, procurement teams and their management, but also any EE, PCB designer, or fabricator involved in PCB specification who wants to know the real-world influences behind the high-speed PCB they “think” they have specified.

This book is written to help you navigate the gulf between the ideal world of your CAD or CAM system and PCB procurement specifications and the physical world of complex processes. We often have to work with non-ideal materials and the limitations of high-speed test and modelling systems, and I believe this book will give you a deeper understanding of where production materials, processes, and test methods deviate from the multi-digit precision that might seduce you into specifying the unachievable. As I often note in my talks, a precision micrometer is of little use when measuring the dimensions of a jelly (jello).

The first step to generating specifications that deliver the boards you require at the most cost-effective price, is acquiring a more intimate knowledge of the tools, materials and processes that go into producing a physical circuit board.

Combined from a series of easy-to-read columns published in *The PCB Design Magazine*, this eBook is written in a way that will benefit PCB designers, engineers and procurement teams with electrical, process or mechanical backgrounds, or anyone who has the desire to learn more about what can and can't be achieved when a suite of CAD layout and its associated stack-up are submitted to the fabrication process.

This book highlights the smoothest way to transition quality designs from prototype through to production from a signal integrity perspective. In the world of signal integrity, the best designers and fabricators measure, model, then measure again to ensure the highest quality predictable signal integrity in their designs and products.

A major topic is the emergence of new silicon families designed to push traditional materials into the multi-gigahertz arena; these new chipsets lift transmission speeds up to a point where signal losses rather than reflections become the predominant concern from an SI perspective. Expanding a little on the topic of transmission line losses, it's worth thinking back to a previous generational shift in high-speed considerations for PCBs.

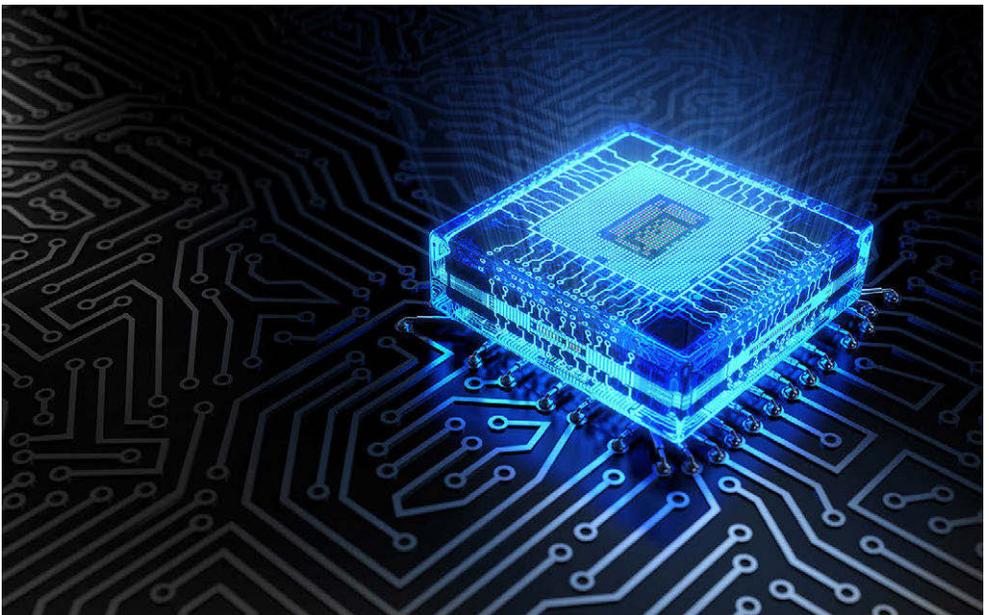
The early 1990s saw the emerging need to consider controlling the characteristic impedance of PCB tracks, something we now casually call "controlled impedance" or "impedance controlled." What happened at that time to make PCB transmission line impedance a driving factor in delivering the high-speed boards of that era? The driving force was the arrival of chipsets with sub-nanosecond switching times. Any interconnect that's long enough at a given speed will exhibit transmission line characteristics, and the predominant characteristic of interest will depend on a mix of factors: the line length, switching speed, conductor characteristics, and the dielectric properties of the insulator carrying the conductor. In 1990s technology, speeds were high enough and traces long enough that without correct impedance matching, reflections could become a significant hindrance to error-free high-speed performance.

Were there losses in the 1990s era PCB signal paths? Yes, but in the majority of cases, the losses were small enough to be ignored. Today, a whole variety of logic families are running at much higher speeds on the same basic interconnect. Now, though impedance matching is still important to ensure maximum energy transfer into the transmission line, designers need to focus less on how much energy will reflect at the receiving end, and more on whether there will be any energy left to convey the signal at all!

At multi-gigahertz speeds, the transmission line materials sap away energy, and the core and prepreg will lose energy as heat, with the loss tangent being the measure of how much heat energy is wasted in the dielectric. From the conductor perspective, the skin effect results in the available copper conductor area for signal transmission being significantly reduced; again, the resistance of this small area of copper for signal transmission results in heat losses.

The fundamental construction of the transmission line and its characteristics have not changed. Simply put, at these higher speeds some characteristics that had a second-order effect at lower speeds now have first-order effects, and other first-order characteristics become second order. Designers and fabricators need to work together to produce the most cost-effective and reproducible designs by stirring all the driving factors into the most cost-effective mix for profitability through the supply chain and fitness for the end-user application.

An intimate knowledge of the interplay between the driving factors and a willingness to communicate along the supply chain will ultimately result in a more predictable and repeatable, yet cost-effective, design. It goes without saying that careful modelling and measurement are key players in ensuring the health of your finished product.





# CHAPTER 1

## **Material Matters or Materials Matter?**

Materials always matter when it comes to PCB fabrication. As designs progress and the industry changes, PCB materials and the specific material characteristics which impact the day-to-day lives of designers, fabricators, procurement specialists and PCB technologists also evolve. Characteristics that could safely be ignored in the past may now creep up and trip you over, catching you unawares. Yet other characteristics which may have been critical on legacy product may only have a second-order influence on your PCB specification and its chances of performing as expected.

Important in guiding you through this are the specialists in the PCB base material supply industry. This industry, which once offered only a selected handful of material choices, now provides a whole range of suppliers providing a complete gamut of materials with a range of purposes. This adds complexity and perhaps confusion as designers, fabricators, procurement specialists and technologists work together to select appropriate base materials. Most material suppliers will have OEM teams to guide you toward the correct base material or family of materials.

### **Choosing Materials**

Knowing what you need is always a good place to start. The choices may seem endless: High Tg or low Tg? Halogen-free? High-speed? Controlled impedance? Is insertion loss critical? Rough or smooth copper, reliability and susceptibility to thermal cycling and thermal stress? Will the PCB go in a short-lived consumer product, or in a satellite, undersea cable, or automotive? Will it face harsh environments? Is it highly price-sensitive, but with a lifespan midway between a mobile phone and aerospace applications?

Will the PCB be laser drilled, sequentially laminated, or HDI and subject to repeated press cycles? Once designed, will the board be produced in low quantities by one fabricator or will it ramp up and be sourced from a volume fabricator in another country? Maybe the OEM will handle procurement directly or, as often happens, the procurement will be outsourced to a specialist broker. What happens to the carefully crafted materials specification as the specification wings its way across the supply chain?

Cost is almost always there to intervene, and getting the PCB specification correct for the specific application—neither over- or underspecified—is important if you wish to minimise the cost for a specific application.

Conversations with technical buyers at trade shows have raised the following question multiple times. “When I send out a PCB spec for quotation, or purchase PCBs from multiple suppliers, why is the construction of the stack-up different from the same stack specification?” In more than one case a technical buyer expressed frustration that the same PCB purchased repeatedly from the same supplier was realised with different material stack-ups. The question is this: Does this matter? And the answer is, sometimes yes, sometimes no, and sometimes maybe. However, the more the procurement team knows of the ultimate application, the better they are able to specify the PCB to an appropriate level.

Let’s look at two extremes of PCB specification and then follow with a checklist to fill in the specification space in between.

At the lowest end, the PCB could simply be a carrier for low-power LEDs for an indicator in machine status lights; the PCB may be wired into the machine, and the PCB fitted with screws to a back-plate. Thickness isn’t critical, and neither is power handling, and the environmental stress on the board could be pretty benign too. Likewise, the volume produced may be low so, really, all that matters is that the board be the correct X and Y dimensions, have holes in the correct places, and the correct Gerbers imaged on the correct layer. It might need to be lead-free or halogen-free to comply with environmental regulations and the minimal specifications required.

At the highest end, consider a large aerospace PCB that must be built by a fabricator with all the correct approvals, and likely from material which is certified for the job too. The layer stack-up will be tightly controlled, and any changes will have to be thoroughly investigated and signed off by the appropriate parties.

In between these two extremes there is far more space for PCB technologists and procurement teams to make intelligent decisions in order to gain the best commercial advantage, and this does not necessarily mean just a price negotiation. A well-specified PCB will help a fabricator get a better yield with appropriately priced materials, with less waste in the process, and everyone wins. Good communication can allow businesses to work together to maximise profits and to minimise scrappage and waste.

**Checklist:**

- Low, medium, high or ultra-high speed?
- Low, medium or high volume?
- Small or large PCB size?
- Short or long high-speed traces? (Shorter traces make life easier for high-speed signals for a given material type.)
- Layer count?
- Sequential lamination?
- HDI?
- Back-drilling?
- End-market: Consumer, industrial, automotive or aerospace?
- Single supplier or multiple sourced?
- Laser or conventional drilled?
- Environmental or other regulatory requirements?

As OEMs, designers and PCB specifiers, you have a range of choices with regard to material specification—and specifically how tightly you want to “lock down” the stack-up design. At one end of the spectrum, you may allow the fabricator or fabricators to free-build the board, giving you

the best flexibility on delivery and cost. At the other end, you may need to specify materials on a per-layer basis to ensure you receive exactly the stack-up you desire. This, of course, has cost and maybe delivery implications, and might also reduce the pool of fabricators able to quote. Some OEMs have taken a middle route, specifying materials on only the critical high-speed layers, whilst allowing more freedom in the rest of the stack-up.

## Understanding Materials

Material is fascinating, and the more you understand, the more you can work with the characteristics rather than fighting with them. Rarely in previous decades did designers have to concern themselves with such matters as glass style and resin contents, but here is an example of just how this has changed.

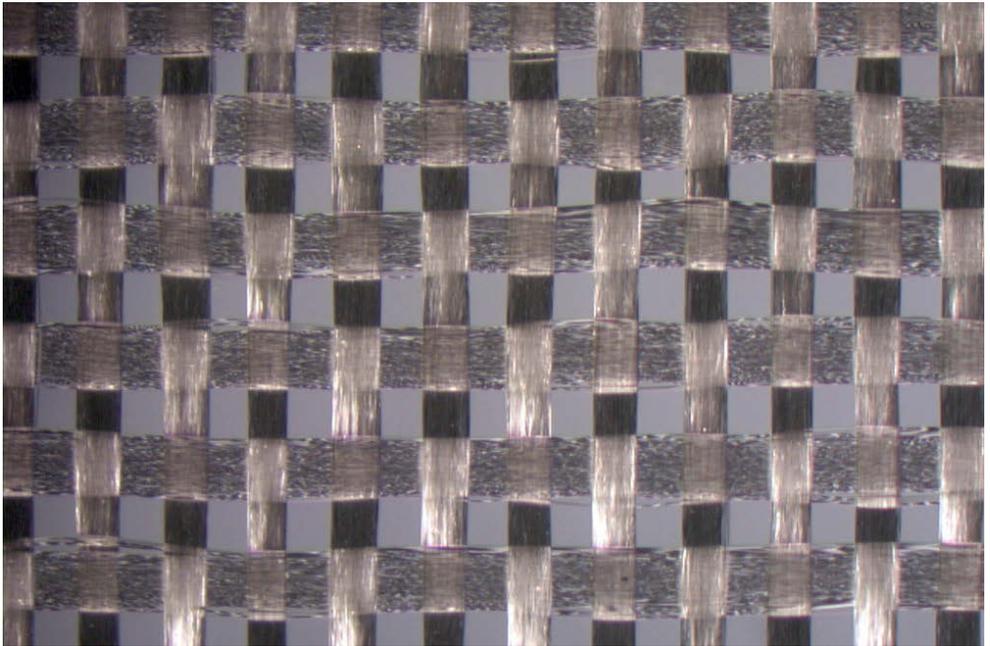


Figure 1.1: Traditional glass cloth / epoxy resin weave (courtesy of Ventec International Group).

Let's take the case of spread glass cloth. You may be aware of a property called fibre weave effect that frustrates high-speed designers. This stems from the fact that glass cloth and epoxy resin have widely different electrical properties.

Park that in your mind and consider something from a completely different arena: laser drilling. When drill companies developed laser drilling for PCBs, the composite nature of base materials limited the precision of laser drilling techniques. You can imagine why: You are trying to accurately ablate holes in a material which is a composite of relatively easy-to-remove polymer and woven e-glass cloth (Figure 1.1), which is not the easiest of materials to ablate. It must be like mechanically drilling into a block wall with steel rebar inserts; the lack of consistency would give even the best mechanical drill a tough time.

On the PCB front, the material suppliers innovated by developing flat or spread glass cloth; this modified the traditional warp and woof (*weft* in the UK) of the fibre and mostly eliminated the gaps in the cloth where the threads cross over. See Figure 1.2.

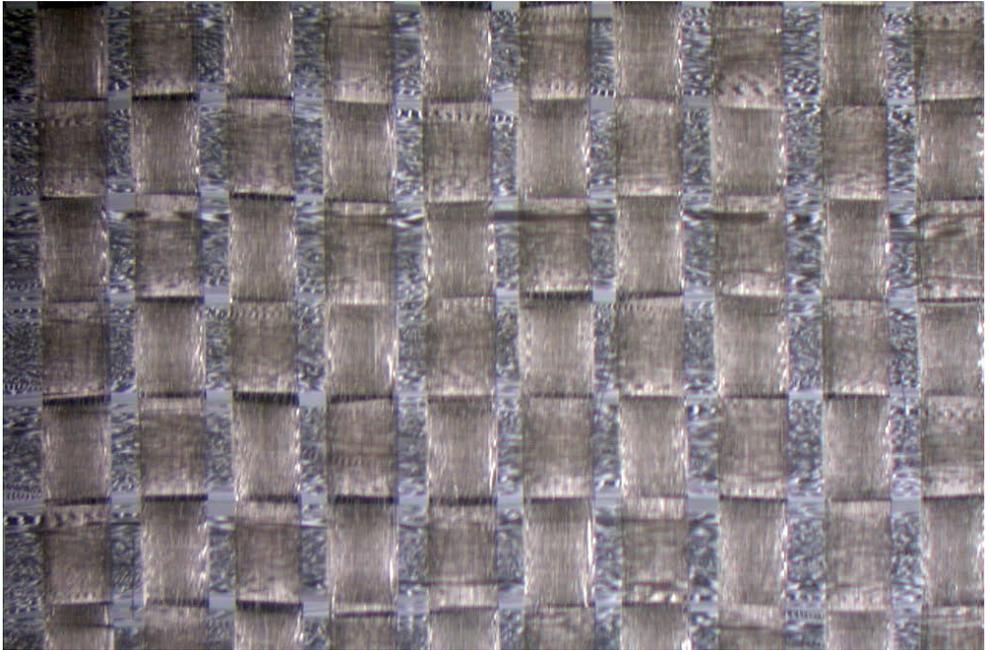


Figure 1.2: Flattened glass cloth/epoxy resin weave (courtesy of Ventec International Group).

This is achieved by mechanical or water jet blasting, sometimes combined with threads that are “low twist,” i.e., the glass yarn has fewer twists per metre, thus making it easier to flatten out. This step function improvement in laser drilling materials has a hidden side effect: the more

even lay of the glass also helps to eliminate the variations of dielectric constant formerly associated with signals transiting along traces that ran predominantly over fibre or resin.

So, the win for drilling presented signal integrity engineers with a win for signal integrity too. There is a “but” coming, which isn’t a problem, but it’s something you should be aware of.

A third benefit of flat glass is that the cloth lies flatter and gives, overall, more control over finished thickness and thickness variation. However, here comes the “but” I mentioned: One benefit of the “old-school” glass styles with the apertures between the crossover of the warp and woof of the cloth is that the apertures allow easy passage of resin from one side of the cloth to the other. So more of the total resin content on top and below the cloth could flow from one side or the other into the gaps between the traces to ensure a reliable lamination process and minimal risk of resin starvation.

For the same resin content, flat glass may prevent the resin from flowing across the glass boundary, so before you change glass styles, you should consult with your material supplier and take advice on the resin content requirements for successful lamination with flat glass. This is not a problem with the material; it simply means that when using the newer material styles, you need to understand what questions to ask to ensure your material supplier can help you specify the optimum build materials.

Next, continuing the theme of communication but with more of an emphasis on the measurement side, Chapter 2 will look at the importance of communication with respect to impedance measuring and modelling.

Layer	Stack up	Supplier	Supplier Description	Description	Stock Number	Type
1		Generic	SMW05	Photimageable Solder Mask	500-004	SolderMask
2		Generic		FR4 HH Core		FR4
3		Generic	FR4 1080 NF	FR4 1080 No Flow		PREPREG
4		Generic	FR4 1080 NF	FR4 1080 No Flow		PREPREG
5		Dupont	FR0110	Dupont FR0110 Coverlayer	800-001	Cover
6		Dupont	AP8525	DuPont AP8525	800-001	Poly
7		Dupont	FR0110	Dupont FR0110 Coverlayer	800-001	Cover
8		Generic	FR4 1080 NF	FR4 1080 No Flow		PREPREG
9		Generic	FR4 1080 NF	FR4 1080 No Flow		PREPREG
10		Dupont	FR0110	Dupont FR0110 Coverlayer	800-001	Cover
11		Dupont	AP8525	DuPont AP8525	800-001	Poly
12		Dupont	FR0110	Dupont FR0110 Coverlayer	800-001	Cover
13		Generic	FR4 1080 NF	FR4 1080 No Flow		PREPREG
14		Generic	FR4 1080 NF	FR4 1080 No Flow		PREPREG
15		Dupont	FR0110	Dupont FR0110 Coverlayer	800-001	Cover
16		Dupont	AP8525	DuPont AP8525	800-001	Poly
17		Dupont	FR0110	Dupont FR0110 Coverlayer	800-001	Cover
18		Generic	FR4 1080 NF	FR4 1080 No Flow		PREPREG
19		Generic	FR4 1080 NF	FR4 1080 No Flow		PREPREG
20		Dupont	FR0110	Dupont FR0110 Coverlayer	800-001	Cover
21		Generic		FR4 HH Core		FR4
22		Generic	SMW05	Photimageable Solder Mask	500-004	SolderMask

Structure Image	Impedance ID	Structure Name	Impedance Signal Layer
	1	Coated Microstrip 1B	1
	2	Edge Coupled Coated Microstrip 1B	1
	3	Edge Coupled Coated Microstrip 1B	1
	4	Offset Stripline 1B1A	4
	5	Edge Coupled Offset Stripline 1B1A1R	4

StackName: Rigid 1	Version: 2017	Revision:	Modification:	Date of Revision:	Editor:	Page 1/2
Date: 27/05/2011	Associated Documents:					
Author: Richard Atwell	Stackup report generated by Polar Speedstack PCB stackup design and documentation system. Stackup courtesy of Printed Circuits Inc (C) Printed Circuits Inc 2013 (c) Polar Instruments Ltd 2013					
Department: Engineering						
Site:						

Copyright © www.polarinstruments.com

Structure Image	Impedance ID	Structure Name	Impedance Signal Layer
	6	Offset Stripline 1B1A	5
	7	Edge Coupled Offset Stripline 1B1A1R	5
	8	Coated Microstrip 1B	8
	9	Coated Microstrip 1B	8

Drill Image	1st Layer	2nd Layer	Column Position	Drill Type
	1	2	2	Laser PTH
	1	8	1	Mechanical PTH
	8	7	2	Laser PTH

Notes  
Stackup report generated by Polar Speedstack PCB stackup design and documentation system. Stackup courtesy of Printed Circuits Inc (C) Printed Circuits Inc 2013 (c) Polar Instruments Ltd 2013

StackName:	Version: 2017	Revision:	Modification:	Date of Revision:	Editor:	Page 2/2
Date: 27/05/2011	Associated Documents:					
Author: Richard Atwell	Stackup report generated by Polar Speedstack PCB stackup design and documentation system. Stackup courtesy of Printed Circuits Inc (C) Printed Circuits Inc 2013 (c) Polar Instruments Ltd 2013					
Department: Engineering						
Site:						

Copyright © www.polarinstruments.com



## CHAPTER 2

# Correlation, Communication, Calibration

It is interesting to stand back every now and then and look at an engineering task from a greater distance. I am always interested in how much some technologies change but how the overall concepts stand still. I once attended an exhibition at Bletchley Park, the UK's WWII centre for code-breaking and arguably the home of computing as we know it (though I am sure that there are similar sites where such original research took place in the U.S., Germany, Japan, France). Alongside the WWII Enigma code-breaking machines stand a collection of computers, many in working condition, that takes the computing story from vacuum tubes (or *valves* in Britain), punched cards and paper tape, through to tablets and flash drives.

How much technology has changed, whilst at the same time, how little progress! More bits, more speed, and more resolution, but the underlying concept has not changed. It's still stored programs (called *routines* in the early days, source of the word "subroutine"), some working memory, an arithmetic and logic unit. The paper tapes are now flash drives, the magnetic cores now static RAM, and the ALUs comprised of vacuum tubes now compressed and implemented in silicon on an unimaginably small scale. At one trade show, Tektronix displayed a 1960s oscilloscope alongside all of the latest models, yet despite the passing of decades, the prospective customers still ask exactly the same questions as they did 50 years ago: "What's the bandwidth? Will it work in my application? How accurate?" And then the predictable "How much does it cost?"

Correlation is a subject that also leads to similar questions, and as production techniques, circuit speeds and the required measurements

have become ever more complex and demanding, it gets harder for a production engineer to track down the source of errors in any situation requiring correlation. The PCB world is no exception. Equipped with sophisticated modelling tools that often present predicted results to many significant places, it can be easy to get lulled into the false illusion, "Because I can predict it, I can produce it."

However, it is important to recall that though modelling tools may be able to predict a result with many decimal places, that ideal can only be realised when "ideal" materials are used. Richard Attrill, our engineering director, recalls the early days of CAM when designers suddenly found the ability to specify hole diameters to many more decimal places than the drills or plating processes of the time could ever dream of achieving.

Sometimes a measurement result is quoted with an emotional statement. "Tell me why your model is wrong as I can't get my measurements to agree." In these situations, step back and look at the materials in use. What is the mechanical tolerance achievable? What is the electrical tolerance? Is the material a composite of differing base material characteristics? Putting all these numbers and their associated tolerances into a Monte Carlo simulation is the only way to truly find if the model is predicting the result to be within the window of possibilities. Table 2.1 and Table 2.2 show the typical distribution of values of impedance of a 90-ohm edge-coupled stripline structure over a range of samples.

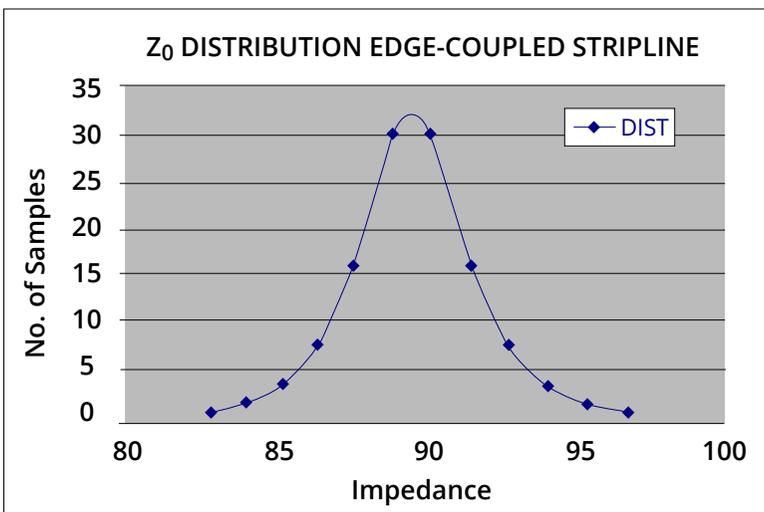


Table 2.1: There will always be a range of possible outcomes when comparing measured with modelled.

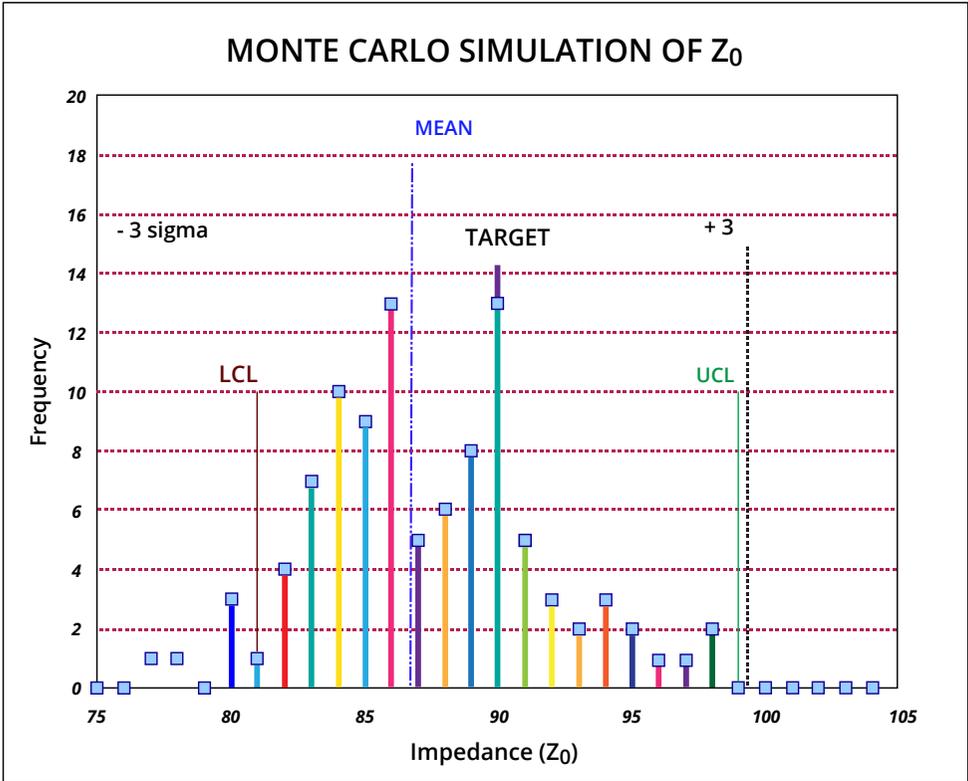


Table 2.2: A Monte Carlo analysis can help predict worst case and most likely scenarios. (Monte Carlo simulations are available for download from the [Polar Instruments website](#).)

A few years back, Dr. Eric Bogatin spoke at a Polar conference. One of the delegates challenged Eric with the following question: “Can you tell me which is more correct, the measured or the modelled answer?” Hopefully, my memory serves me correctly, but as I recall, Dr. Bogatin said, “Neither. Think of the measured and the modelled answer as being in a dance, drawing ever closer as the dance progresses. The model first gives you an area to shoot for in your measurement: if the measurement is close, then adjust your model to see if you can get a better prediction, and then see if you can fine-tune the measurement until your measurement and model converge into the level of accuracy you desire.”

Thinking along similar lines, keep in mind the well-known quotation by George E.P. Box, professor emeritus of statistics, University of Wisconsin: “Essentially, all models are wrong, but some are useful.” In other words, any prediction or measurement should be taken in conjunction with

statistical analysis to predict the probable range of outcomes. In the area of modelling and measuring impedance on PCBs, it is worth having a checklist of items that may influence the measured and the modelled outcomes.

Bear in mind also that sometimes when a specification has been communicated through a non-technical channel or a non-specialist channel, the specifications may have been tightened beyond achievable limits by people with a non-engineering background. This sometimes happens when a management team is overzealously implementing a quality improvement plan. These teams sometimes issue edicts without thinking through the consequences; e.g., "To reduce quality problems we have asked suppliers to make specifications twice as tight." It really shouldn't happen but sometimes it does. When I encounter a Polar customer looking for an impedance specification on an FR-4 PCB that is tighter than that of the uncertainty on a precision reference air line standard, bells start to ring that the specification has gone through some adjustment by non-specialists in the field.

Consider the two following checklists of factors applicable when modelling and measuring impedance on PCBs:

**Checklist for modelling impedance:**

- Dielectric height variation?
- Line width variation?
- Resin content variation?
- Resin rich areas?
- Correct ground plane layout?
- Dielectric constant?
- Etch taper?

### Checklist for measuring impedance:

- Equipment calibrated for impedance?
- Traceable impedance standards?
- Coupon design?
- Coupon launch?
- Coupon length?
- Probe quality?
- Cable condition?
- Correct cable type?
- Measurement region?
- Equipment normalised for temperature?
- Hands and materials away from microstrips?
- Bottom side microstrips lifted from work surface?
- Cell phones off in test area?
- ESD precautions in place?

Whilst these checklists are generated with respect to impedance correlation, the same considerations hold true for any measurement and modelling challenge. I'm certain the questions and answers delivered remain broadly the same as those posed by engineers and metrologists in the early days of the industry.

Still on the theme of measurement, the next chapter takes a deeper look into the sources of impedance measurement error.



## CHAPTER 3

---

# Zen and the Art of Accurate Impedance Measurement

\* – with apologies to Pirsig

In his 1974 philosophical novel “Zen and the Art of Motorcycle Maintenance,” Robert M. Pirsig contrasts his ongoing daily approach to motorcycle maintenance with his friend’s alternate view of leaving well enough alone between annual service center-based maintenance. What has this got to do with accurate impedance measurement, you may ask? Please read on. While I am writing this with the aim of fine-tuning your impedance measurements, the underlying principles hold true for any type of measurement.

When measuring impedance with any type of TDR or impedance test system, we face a number of sources of potential measurement error. This chapter sets out to explain those error sources and how you can minimise them in order to achieve repeatable and accurate measurements. First, let’s consider probes and probing, which can be the Achilles heel of any measurement. You should look for a probe which has a good RF match to the test cable and has good signal integrity at the launch of the test trace. Some lab probes are superb from an RF perspective, but in a production environment you should also look for adequate robustness to survive the rigorous nature of repeated testing.

Thinking next of calibration, TDRs used for impedance measurement are precision RF measurement tools and need to be annually calibrated. Reference air line standards are used for TDR calibration and are available in a variety of standard impedances. Precision air lines are a high-cost item, so an acceptable alternative for less critical applications is a set of

precision semi-rigid cables calibrated against air lines. Air lines are made traceable by a precision metrology technique called *air gauging* which allows the internal bore of the air line to be measured and the impedance calculated using a standard formula traceable to national standards.



Figure 3.1: Traceable reference air line alongside impedance test probes.

**Hands off:** Resting your hand or fingers on a test coupon will cause the impedance of surface structures to drop. Ensure that operators are aware of this effect. It's easy to demonstrate: simply make multiple tests on a surface trace and see how placing your fingers on the board surface alters the measurement. An extension of this source of error occurs if you test a bottom surface trace when the coupon is in contact with the work surface. Yes, even the work surface can influence measurement results. The work surface has its own dielectric constant and a microstrip on the bottom of the test coupon or PCB will measure low if it is too close to the table surface. There are two ways to resolve this: Place the coupon in a test fixture or support jig, or turn the coupon over so the bottom layer faces up.

**Secrets of TDR calibration:** Many TDRs exhibit a characteristic in which calibration will only be correct if your TDR is calibrated with the same DC conditions at the end of the test cable as those occurring when you measure. Simply stated, if you calibrate a TDR using a precision broadband resistor as a standard, you should also terminate your test sample (coupon) with the same resistance. However, if you calibrate or verify your TDR with an open circuit standard such as an air line you should measure your test sample without resistive termination. As it is inconvenient to fit a terminating resistor to a test coupon, always calibrate a TDR used for coupon testing with an air line or precision semi-rigid reference. The error between the two methods can be as much as 3 or 4 ohms. The reason behind this effect is that TDR sampling heads are precision fast-switching diode bridges and they are sensitive to temperature change. A change in DC conditions at the test sample will alter the DC output voltage of the pulser.

**Worn cables and probes:**

RF cables and probes have a finite life and should be regarded as consumables. With 24/7 operation, they will, in time, become resistive and ultimately fail. Cable life can be extended by careful handling, avoiding tight bends, etc. Operators should be trained to take care of cables and not to wrap them tightly against the probe or flex them more than necessary to make tests; taking care of cables will help ensure accuracy is sustained between annual service and calibration. Avoid falling into the trap of one PCB fabricator whose well-meaning operator intentionally used worn probes to help a batch of “out of spec” boards pass testing!



Figure 3.2: New vs. worn SMA connector—result of many thousands of connections & disconnections, or being rotated whilst not fully torqued tight.

**Drift:** Some TDRs are susceptible to measurement drift over time and temperature. Ask if your TDR makes compensation automatically for this; i.e. is compensation inbuilt? If your TDR does not have inbuilt compensation it may be necessary to verify measurements if the temperature of the test environment varies significantly during the day.

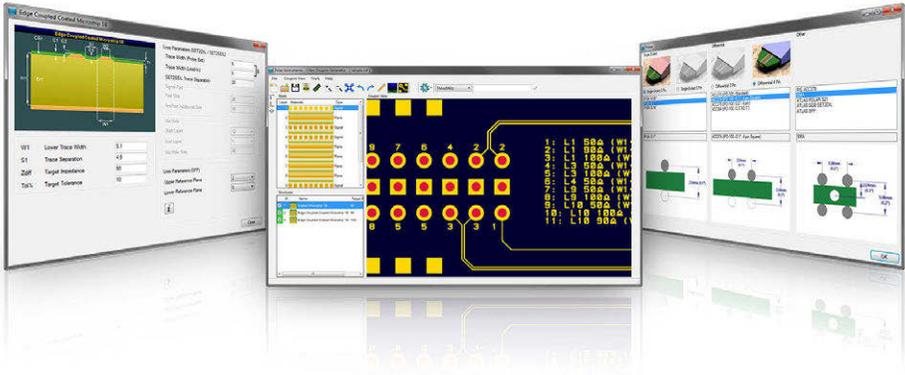
**Cell phones:** Are cell phones influencing your measurement? Cell phones are RF transmitters and regularly “sign on” to the nearest base station,



even when you are not making a call. Test coupons are around the same length as a mobile antenna and will readily receive the signal from your phone. This is especially the case with surface structures like microstrip, so do ensure phones are switched off in the test area.

**Test coupons:** Test coupons provide a reliable way of verifying PCB impedance and will offer you more reliable repeatable measurements than attempting to measure the board itself. The advantages of using test coupons are described in detail on the Polar [website](#). *Important note:* If your striplines are reading high, did you remember to short the planes Vcc and Gnd on the coupon? (No, *NOT* on the board!) Vcc and grounds need to be shorted on the coupon—especially on narrow coupons—to simulate actual RF conditions on the finished board. *Tip:* If increasing the height of the top plane to 10x its normal height on your field solver gives you a reading of impedance similar to your measured value, you have probably forgotten to short circuit the planes on the coupon.

Last, but not least, is the area of protection against ESD damage. The faster the rise time of your TDR system, the more care needs to be taken in this area to keep running costs to a minimum and in order to avoid cumulative damage to its sensitive input circuitry.



Back to “Zen and the Art of Motorcycle Maintenance.” Whilst Pirsig points out the wide difference between the two approaches to maintenance (frequent ongoing minor adjustment vs. longer interval-based “central servicing”), the highest-quality results are obtained when both methods are used together and the user is sensitive to day-to-day changes in performance.

After reading about these sources of measurement error, you can see how keeping impedance test operators well-trained and attuned to the variations caused by cable damage or other degradation will ensure maximum confidence in your impedance measurements during the full interval between routine calibrations.

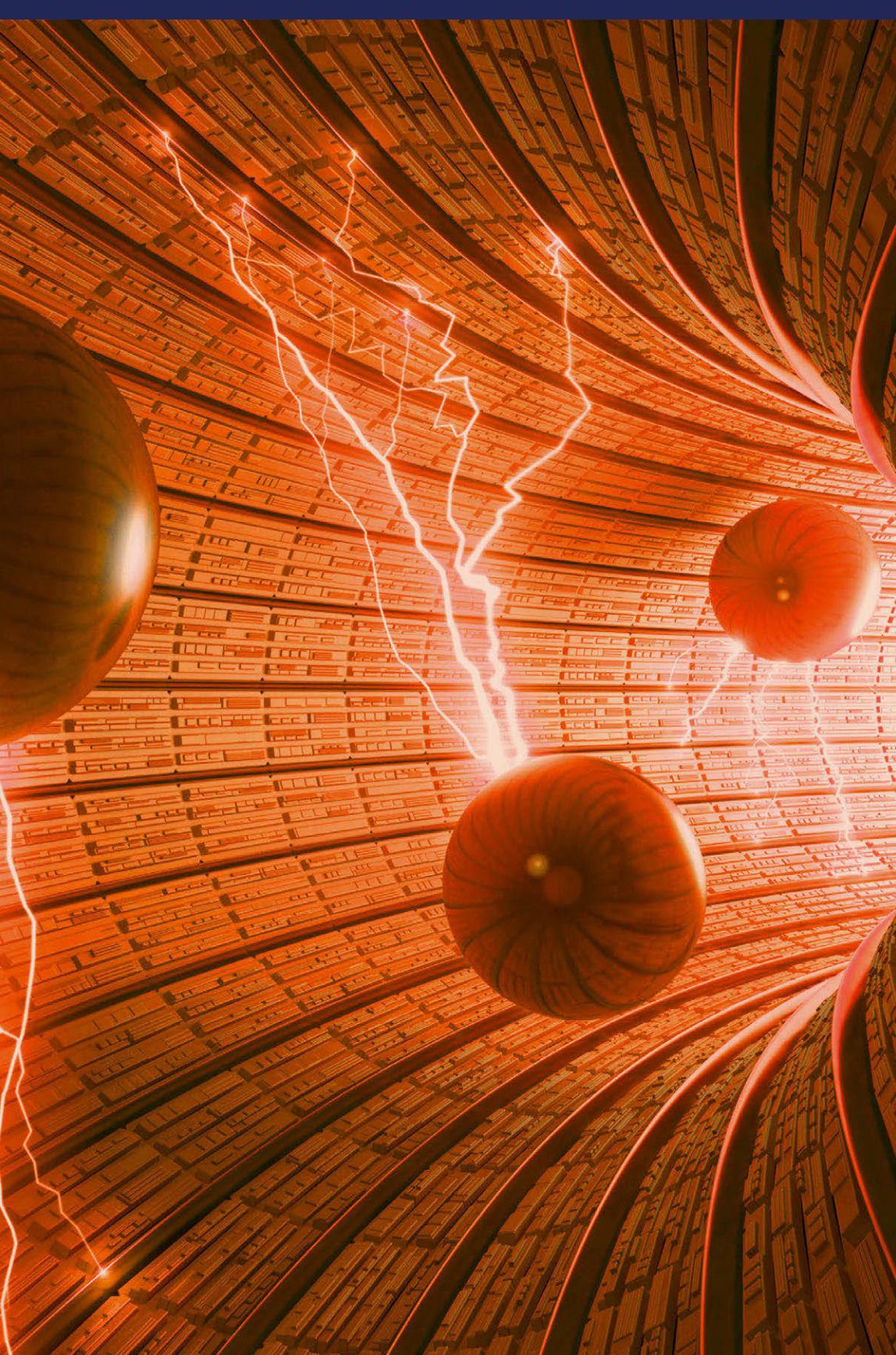
By the way, Pirsig’s book sold over 4 million copies in 27 languages and was described by the press as “the most widely read philosophy book, ever.”

According to Pirsig, despite its title, “It should in no way be associated with that great body of factual information relating to orthodox Zen Buddhist practice. It’s not very factual on motorcycles, either.”

It’s now time to take a look at what happens outside of the band of frequencies where the line behaves broadly independently of frequency.

## Reference:

\* Robert M. Pirsig – “Zen and the Art of Motorcycle Maintenance,” ISBN 0-688-00230-7



## CHAPTER 4

# Transmission Lines: A Voyage From DC —No, Not Washington, Part 1

In these next two chapters, I'd like to take you on a voyage through a transmission line from DC onwards and upwards through the frequency spectrum. Step by step, we will explore the characteristics through the dizzying rise from very low to ultra-high frequencies. But, rest assured, I won't go beyond what is of practical use to you right now. In Part 1, we will trace the impedance from infinity at DC to the GHz region where it reaches the steady state value of its characteristic impedance.

I must start with a confession to long-time followers of Polar's website; many are process and chemical engineers for whom electronics is not their specialised subject. If you have read Polar applications notes or been to our seminars, you have probably heard us say time and again that impedance is frequency-independent. Well, it's much like how you learned in elementary school that the molecule was the smallest entity, and then you went on to high school to find that atoms were smaller, and a couple of years on you realise that atoms actually comprise protons, neutrons and electrons, and then you entered the realm of quarks, muons and mesons, strangeness and charm. Well, the story we taught at Polar was true, but *only* under a certain range of conditions.

So now, it's time to tell you the whole story, or rather the whole story up to just above the frequencies that are relevant today.

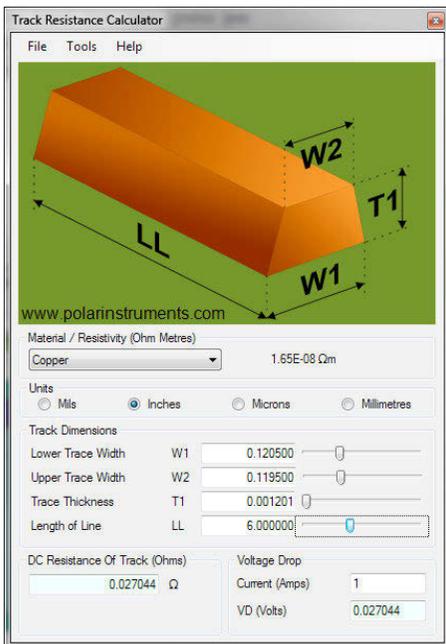
PCB process engineers took our word for it that a 6-inch (150 mm) coupon comprised of a narrow trace located a fixed height above a wide ground plane had an impedance (often of 50 ohms), but I am sure only half of them believed us. If you measure resistance between the trace and ground with a digital multimeter, the circuit has infinite resistance!

So, what is really going on here? Another puzzle to new customers is that measuring the resistance of the trace from one end to the other shows a short circuit, or an almost short, a NAD (near as dammit, as my math teacher used to say).

I can hear you saying, “So, tell me the truth then!” Well, the truth is that at different frequencies all the transmission line characteristics have influence on line behaviour in differing ways, some of them surprising and some counterintuitive. When reading this chapter, it is important to remember that *characteristic impedance* is an inherent property of the line itself and is unchanged regardless of input or output impedance. The *input impedance* (which is what is seen by a TDR or a VNA) is altered by termination source and load, and the length of the line itself.

## The Transmission Line at DC

Let’s begin at the start, nice and easy, with 6-inch long line, FR-4 substrate at DC. For ease of visualisation, imagine a line designed for a 50-ohm characteristic impedance on a 63-mil (1.6 mm) thick, double-sided board. Just take it as given that the trace needs to be around 130 mils (3 mm) wide to make a 50 Ohm characteristic impedance line. Measure the resistance between the trace and ground with a simple digital multimeter—and it reads open circuit.



Let’s consider two ways of looking at the line: one by measuring the characteristics of the line when “looking into” the signal and ground lines, and the other by looking at the resistance of the signal trace itself, i.e., measuring the resistance between the start (0 inches and 0 mm) and the end of the line (6 inches ~150 mm). In both instances, we’re using the dimensions of a typical trapezoidal profile PCB copper trace.

Figure 4.1: Track resistance of 6-inch trace.

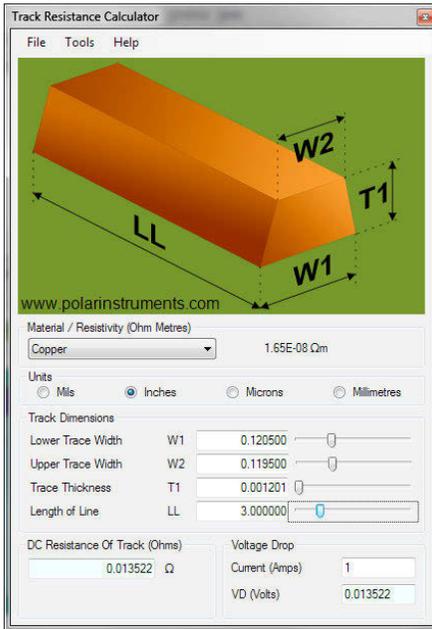


Figure 4.2: Track resistance of 3" of trace.

At DC, an unterminated impedance-controlled trace with a *characteristic impedance* of 50 ohms actually has an open circuit *input impedance*.

From the calculation in Figure 4.1, you can see the end-to-end resistance of the trace itself will be about 27 milliohms, or small enough to be ignored.

Just for interest, halfway down the trace (line length 3 inches  $\approx$  75 mm) the resistance is 13 milliohms, as seen in Figure 4.2, so there is a linear relationship between resistance and the length of the trace. That might seem obvious but keep this in mind for later.

## Increasing the Frequency

Next step is to start ramping up the frequency and see what happens. Going back to physics, at low frequencies a length of copper over a ground plane separated by an insulator (the FR-4 base material) would seem to be like a capacitor, and at low frequencies it behaves just in that way. As the frequency ramps up, the impedance steadily falls from infinity.

Look closely at Figure 4.3 on the next page. You'll notice in the KHZ decade that you can see the input impedance magnitude falling rapidly from its DC value of infinity. However, you can also see that, unlike a pure capacitor whose impedance magnitude you would expect to fall to a negligible reading at higher frequencies, something else seems to be slowing the rate of decline in impedance magnitude. The picked data point on the graph at 1 MHz shows an impedance of 52 ohms. So, what could be causing the graph to flatten out?

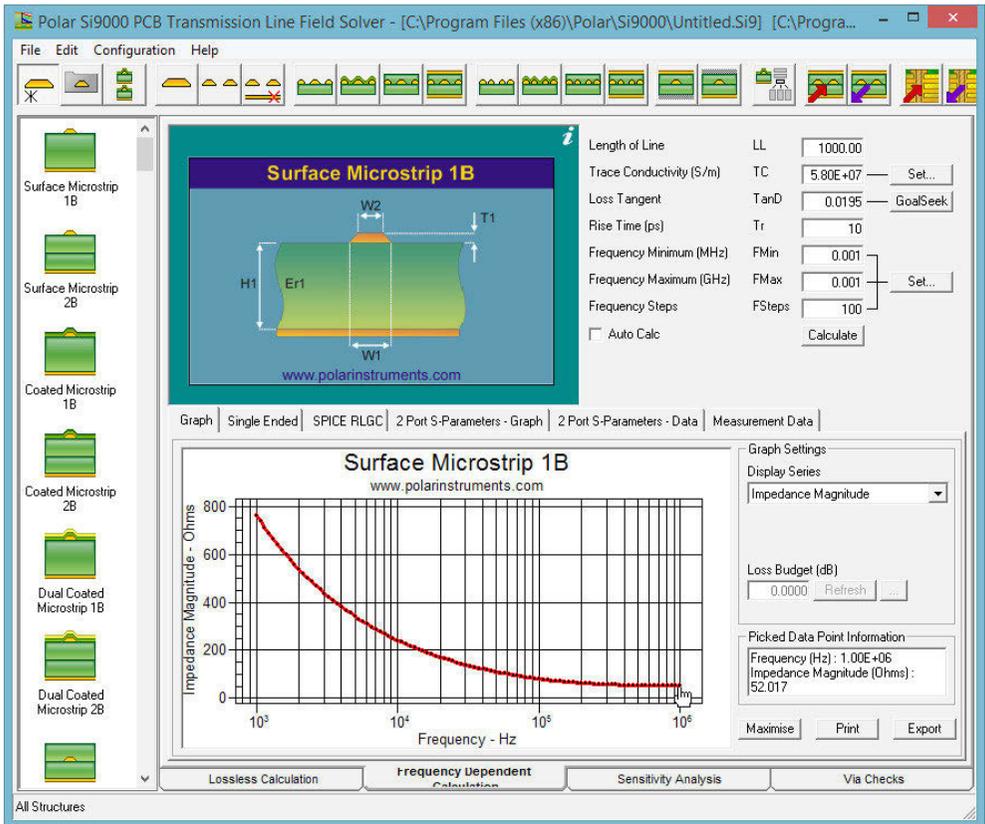


Figure 4.3: Note that the impedance magnitude falls rapidly from its DC value of infinity.

## Impedance Frequency-Independent?

Back to basics here. For the past couple of decades of Polar seminars, we have explained to fabricators that the PCB characteristic impedance for lossless lines is equal to  $Z_0 = \sqrt{L/C}$ . Well, I'll let you in on a secret: That information was accurate, but only accurate over a band of frequencies commonly used at the time. With ultra-high-speed serial transmission, designers have become preoccupied with very high and, somewhat counter intuitively, lower frequencies. You're thinking, "Why lower?" Well, for example, ultra-long streams of data comprised of all zeroes or ones represent a much, much lower frequency than the clock rate. This is why bit error rate test (BERT) testers deploy very long data words with a pseudo random series of highs and lows to represent the broadband nature of high-speed serial data transmission.

I digress; let's go back to the equations for a moment. For lossless

lines operating from a few 10s of MHz to one or two GHz the above approximation worked just fine, and the lines operated in that region behaved reasonably independently of frequency.

However, the full equation for transmission line characteristic impedance is:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

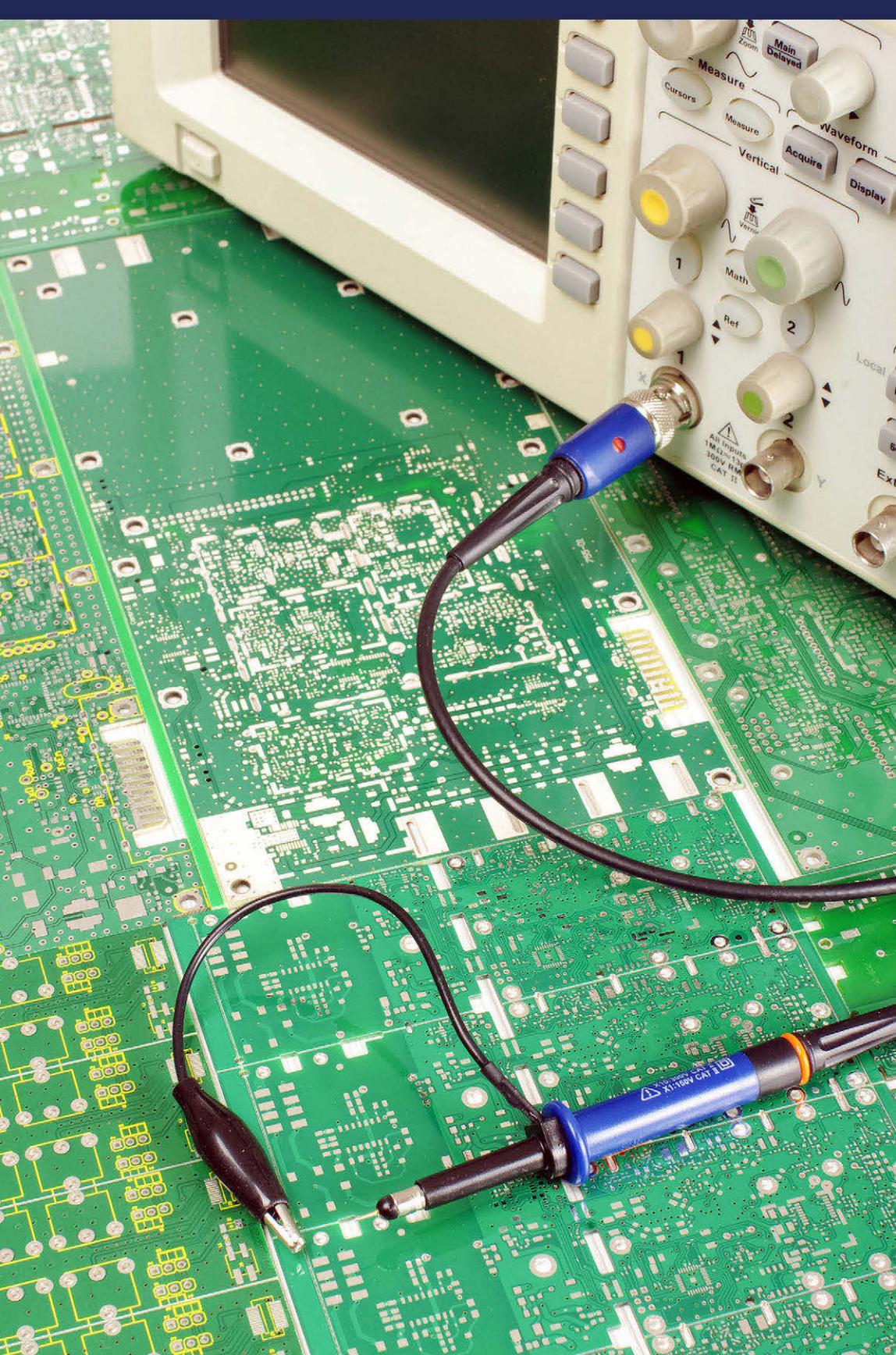
Let's look at the low-frequency case first and have a think about these terms. We have already learned that at mid frequencies, R is small enough to ignore and G (the conductance of the substrate) is also small enough to ignore. But as the frequency falls, so does the inductive reactance, and gradually  $j\omega L$  becomes small making R significant. As this starts to happen, the line impedance becomes frequency-dependent and the impedance equation shifts to a point where  $j\omega L$  can be ignored but R cannot. The impedance in this low-frequency region tends toward:

$$Z_0 = \frac{R}{j\omega C}$$

Push the frequency higher and as  $j\omega L$  grows large compared to R, then the line behaves in a frequency-independent manner as the  $j\omega$  top and bottom cancel; the instantaneous impedance reaches a reasonably steady state.

Important points: *Characteristic impedance* and *input impedance* are not the same. The characteristic impedance of a line is an inherent property of the line itself and is unchanging regardless of how the line is driven or terminated. Input impedance, however, changes according to both the source and termination of the line. Measurement systems and interpretation are designed to allow you to "see" the impedance of the line itself if they are properly interpreted so it is important to understand the difference between the two. And if you don't, ask!

The next chapter, Part 2, will look at other mechanisms that introduce loss into the line, draining the signal of its energy as it transits the line.



## CHAPTER 5

# Transmission Lines: A Voyage From DC —No, Not Washington, Part 2

In the second part of this two-part series, we continue on our voyage through a transmission line from DC onwards and upwards through the frequency spectrum, step-by-step exploring the characteristics from very low to ultra-high frequencies. In Part 1 we charted the impedance from infinity at DC to the GHz region where it reaches the steady state value of its characteristic impedance, in this case 50 ohms. Part 2 looks at mechanisms that cause loss in the line, robbing the signal of its energy as it transits the line.

On the next page, Figure 5.1 shows the impedance magnitude flattening out at 50 ohms in the range of 1GHz through 20GHz.

So, that takes us from DC to the GHz region, and we have seen so far that the characteristic impedance falls from infinity at DC to a steady state of 50 ohms and flattens out.

Surely something else must happen at higher frequencies. Everyone asks about line performance as data rates loft into the multi GHz region. Whilst the instantaneous impedance stays roughly constant, the line can no longer be treated as lossless as a range of loss mechanisms come into play to attenuate the signal.

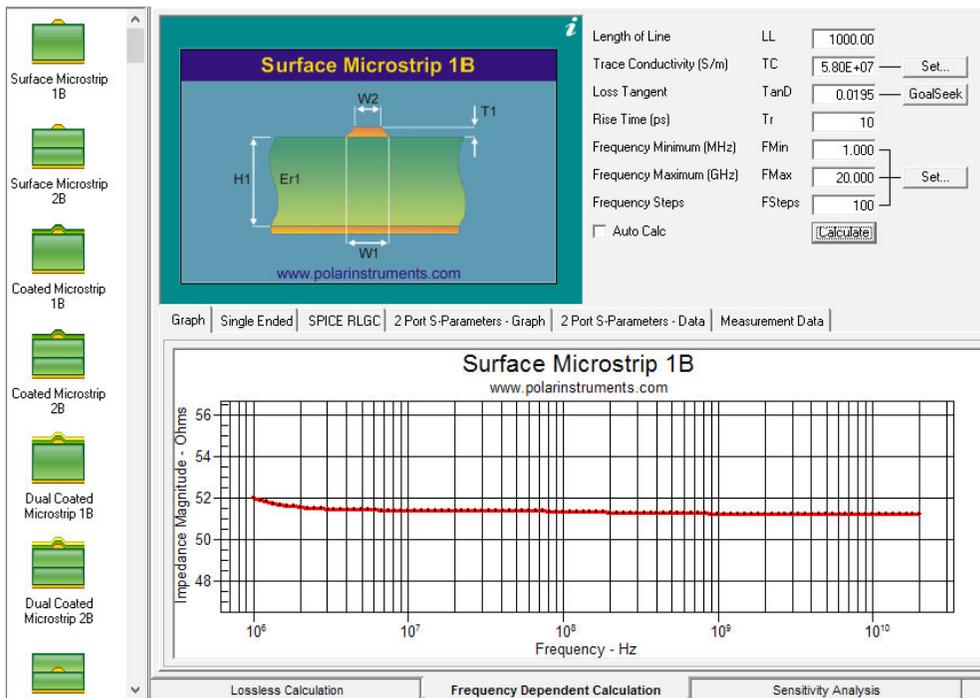
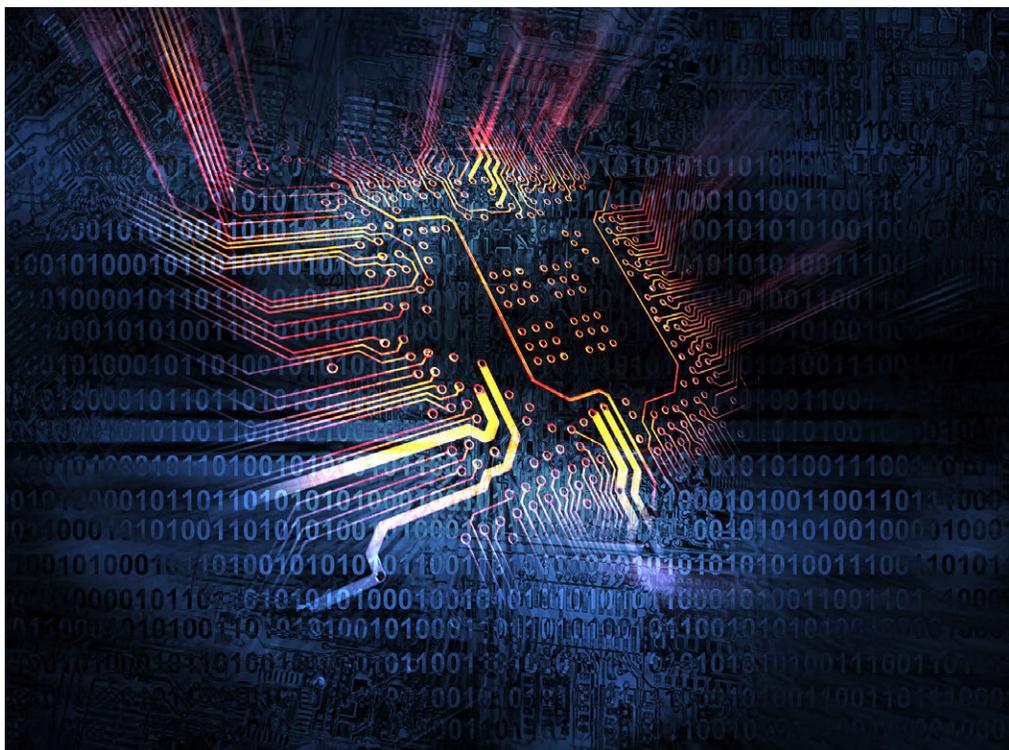


Figure 5.1: This image shows the impedance magnitude flattening out at 50 ohms in the range of 1GHz through 20GHz.



# Skin Depth

Skin depth is the first loss mechanism that must be taken into account. As the frequency is increased, currents increasingly flow on a thinner layer closer and closer to the surface of the trace; this reduces the effective cross-section available for current flow, and hence the AC resistance increases and becomes frequency-dependent until the point where almost all the current is flowing on the surface of the trace. Figure 5.2 shows that even at the relatively modest frequency of 100MHz, the skin depth of current flowing in the conductor is only penetrating to a depth of approximately 7 microns. At 1GHz, it is down to a single micron, only a tiny fraction of the available conductor.

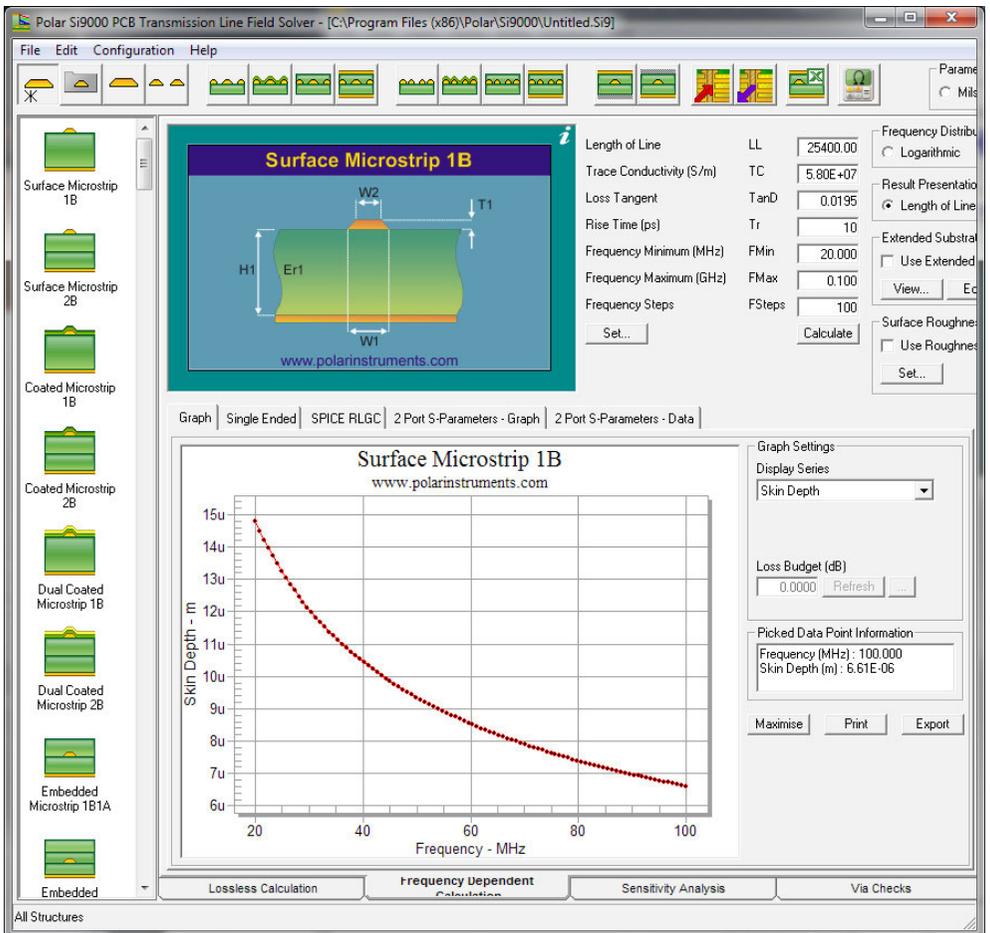


Figure 5.2: Skin depth.

Figure 5.3 shows that at around 100MHz on this structure, the overall losses are still relatively low and that conductor losses are approximately double the dielectric loss.

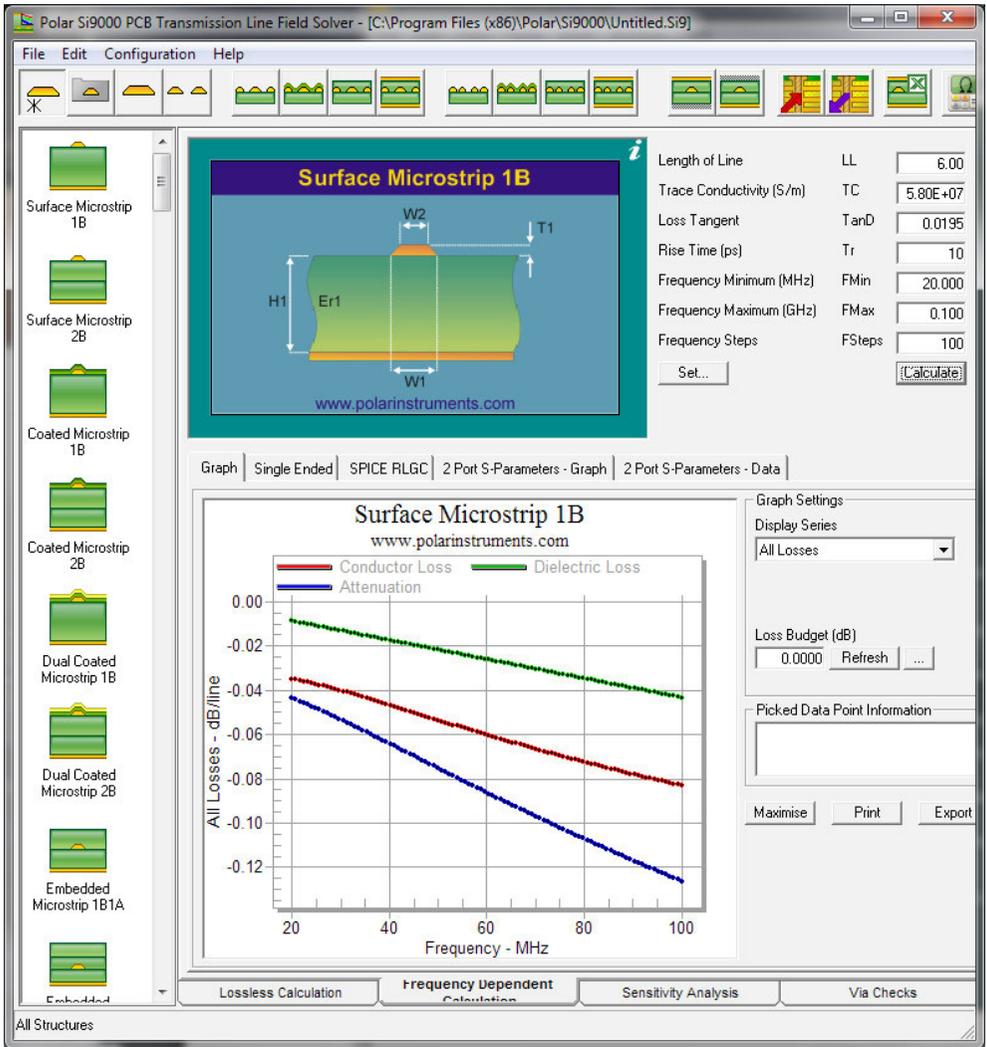


Figure 5.3: Overall losses are still relatively low, around 100MHz on this structure.

Now ask yourself: What needs to happen to the copper to promote adhesion? Typically, the surface is roughened, and given that all the current is flowing on the surface of the trace, the copper (Cu) roughness adds a second hit and robs the signal of yet more energy, as shown in Figures 5.4 and 5.5.

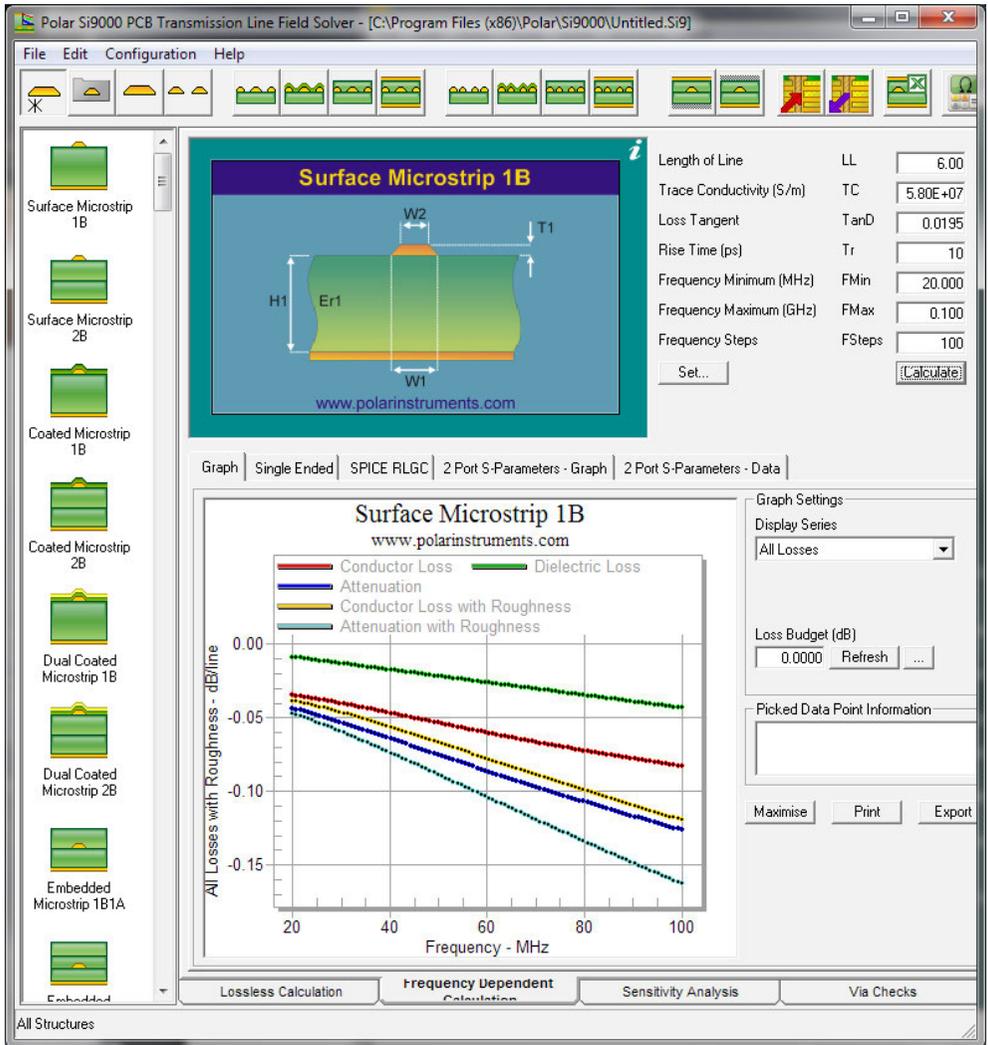


Figure 5.4: Losses with roughness.

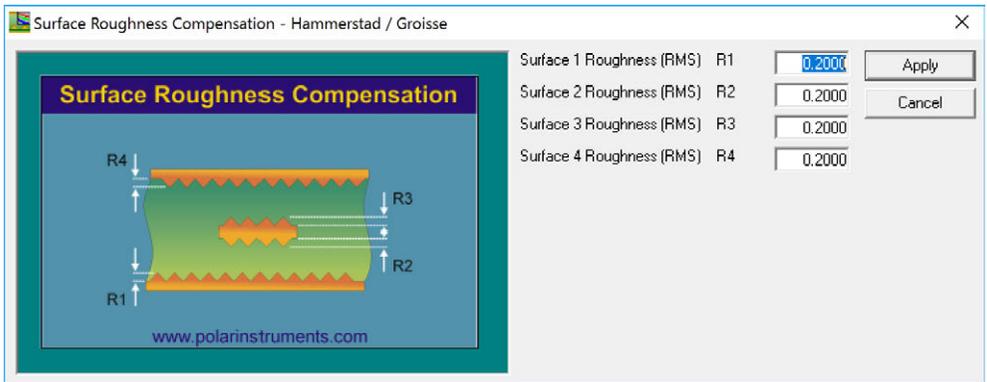


Figure 5.5: Specifying RMS roughness.

A 5-micron RMS roughness (Figure 5.5) almost doubles the amount of conductor loss at the above frequency (Figure 5.4), but as we journey on up the frequency band the skin effect losses, though continuing to increase, only increase in proportion to the square root of the frequency.

## Dielectric Loss

However, the dielectric losses, which are present but at very low levels at the above frequency, increase relentlessly and in direct proportion to frequency, meaning that as you move upward, the dielectric losses ultimately become the predominant loss mechanism. Dielectric loss is the heat energy lost as the substrate charges and discharges; there is a vast range of base materials available from very lossy to ultra-low loss. But regardless of the material, there will be at some point a place where dielectric losses become the main loss mechanism; obviously, this shift is at much higher frequencies with low-loss materials.

Figure 5.6 shows this in graphic detail. For clarity, I have removed the surface roughness effect from the graph. You can clearly see that, as the frequency heads up to 100GHz, out of 8dB per inch of loss, only 0.4dB of the contribution is from conductor losses, the remainder is dielectric loss.

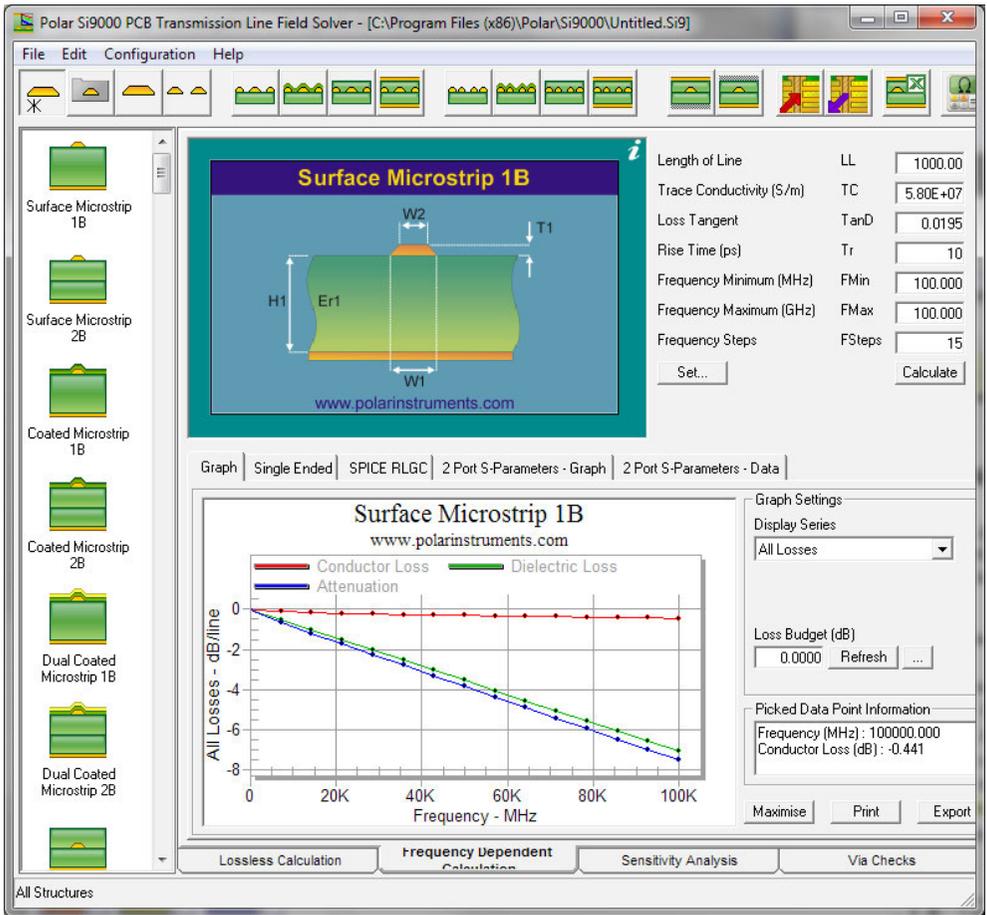


Figure 5.6: Dielectric and conductor loss.

So, there you have it, from DC to 100GHz. I think that is quite far enough for the moment, but if this has whet your appetite for a deeper understanding, I would thoroughly recommend the following references.

In the next chapter, we take a look at how to interpret a specification and the questions you should ask when anyone says, "I need to test this line at 10GHz."

### References:

Dr. Eric Bogatin: "Signal Integrity Simplified," Prentice Hall, ISBN 0-13-066946-6

Dr. Howard Johnson, Dr. Martin Graham: "High-Speed Signal Propagation – Advanced Black Magic," Prentice Hall, ISBN -13-084408-X

Stephen Hall, Garrett Hall, James A McCall: "High-Speed Digital System Design," John Wiley & Sons, Inc., ISBN 0-471-36090-2



## CHAPTER 6

# When Is a 10GHz Transmission Line Not a 10GHz Transmission Line?

A simple question, surely. But there could be a whole host of answers, and by now you will probably be anticipating my answer: Yes, “It depends.” As John Allen Paulos might say, in electronics, uncertainty is the only certainty there is.

Surely 10GHz is always 10GHz, correct? Well, let’s take a look at marketing “spin” first. Often, chipset documents and PCB specs refer to the data handling capability of a link. But not in all cases. For example, a 22Gb/s link may be a pair of 11Gb/s channels, or even four parallel 5.5 Gb/s channels, and if you take into account that data can be clocked on the rising and falling edges the clock rate could actually be 2.25GHz. Suddenly, that brings what seemed like a fantastically high frequency down to “real world” levels.

So, as a fabricator, you really need to dig under the headlines and work with the designer to find the true nature of the channel under test.

A frequently asked question at Polar is, “Can I check my 1, 2, 5, 10, or 20GHz PCBs with a TDR?” The answer is, again, “It depends.” The “it depends” part involves asking whether the line under test exhibits significant losses at the frequency under test or not. If the line length and operating frequency, along with the laminate type when modelled, predict insignificant losses, then the impedance of the line is relatively frequency-independent above a few megahertz. Provided a suitable length test trace is available the impedance can be tested with a TDR with a rise time anywhere between 15ps and 250ps, the only caution being that the faster rise time, in general, will require more care over ESD protection.

However, if the line in question, when modelled, exhibits significant dBs of loss, then a simple TDR test (regardless of rise time) may prove inadequate. In this case a fuller analysis of line behaviour is required, including examining the losses with respect to frequency. This can either be performed with a vector network analyser (VNA) or with a TDR with post processing software required to extract the frequency domain information, along with the line losses. A variety of techniques are proposed in IPC TM-650 Test Methods Manual.

Often PCB fabricators are confused when first confronted with impedance. "Surely this coupon has an open circuit at the end, so the impedance must be infinite." And at DC this is true; however, for any transmission line, the impedance rapidly falls from infinity to a steady state defined by the equation in Figure 6.1:

$$Z_0 = \sqrt{\frac{L}{C}}$$

Figure 6.1: A simplified expression for lossless impedance.

This is clearly shown by the following model which extends the impedance-solving of the line from 10KHz up to 10GHz.

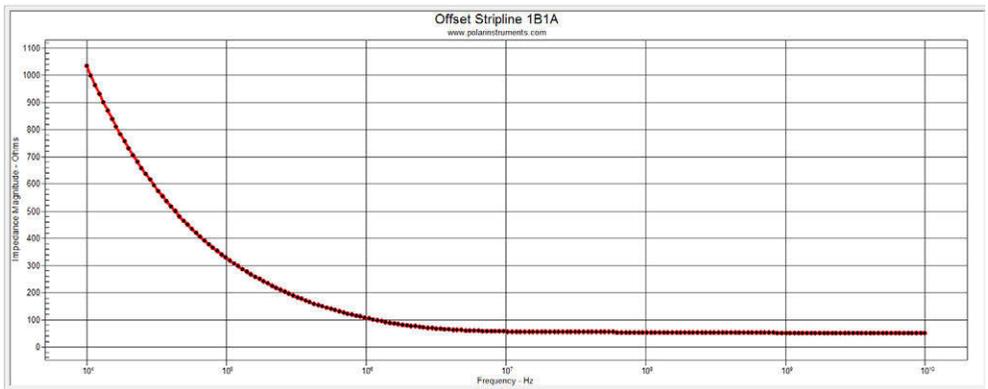


Figure 6.2: A 50-ohm line showing Zo headed for infinity at DC.

Here, modelling is extended to 100GHz:

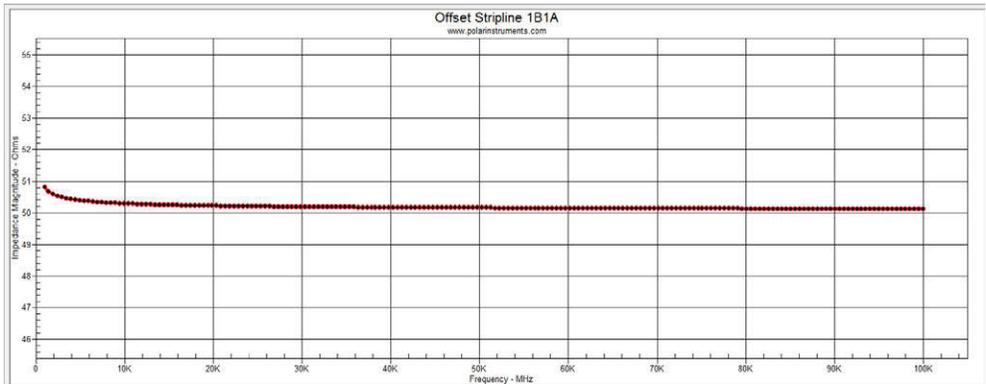


Figure 6.3: A 50-ohm line showing  $Z_o$  between 1GHz and 100GHz.

From these two graphs, we can see the instantaneous impedance remains roughly the same from 10MHz to 100GHz, so what else is happening as the frequency increases?

Whilst the instantaneous impedance stays the same, the increasing frequency leads to increasing losses. Below 2GHz, even on FR-4, most lines of 4 to 5 mil width on ½ oz. copper may be considered lossless, i.e., the losses incurred are small enough to be ignored and these lines may be measured on conventional TDR equipment. Above 2GHz, losses may become more significant; this can be down to the copper dimensions, copper roughness, and the type of dielectric material employed. Again, modelling can be employed to check if the transmission line in question is “in harm’s way” when losses are considered.

Figures 6.4, 6.5, and 6.6 illustrate the conductor, dielectric and total losses for 3-inch and 6-inch lines on FR-4.

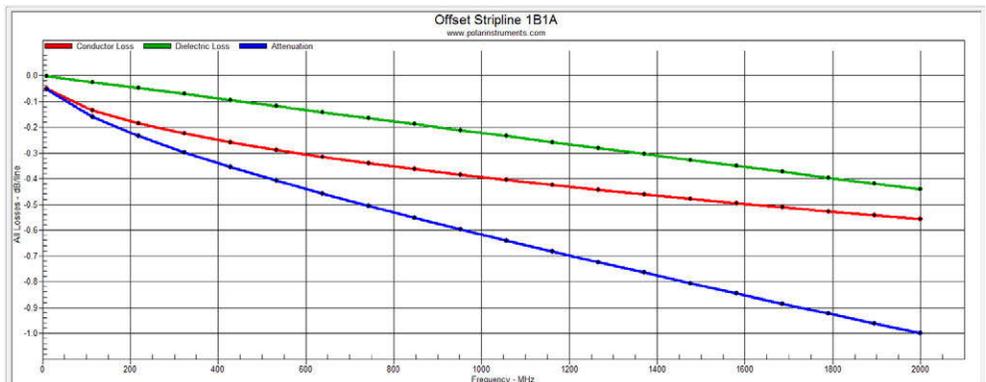


Figure 6.4: This 3-inch line on FR-4 has only 1dB of losses at 2 GHz.

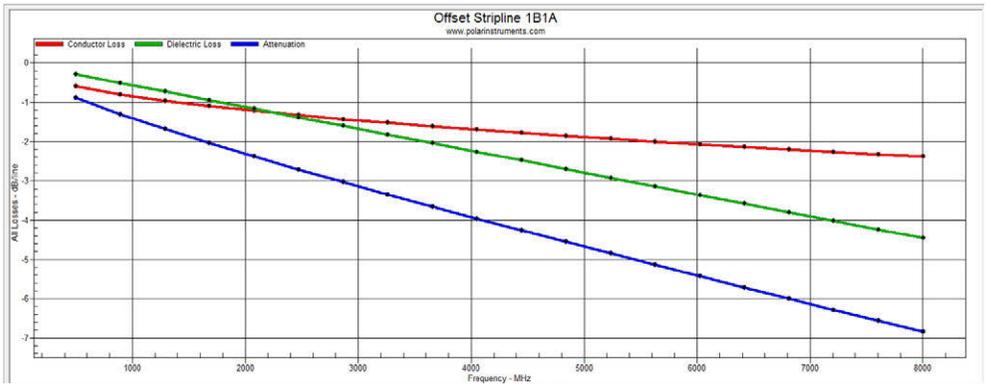


Figure 6.5: This 6-inch line on FR-4 has over 6dB of losses at 8 GHz.

The graph of the same structure below charts the conductor and total attenuation losses when the copper surface roughness is taken into account.

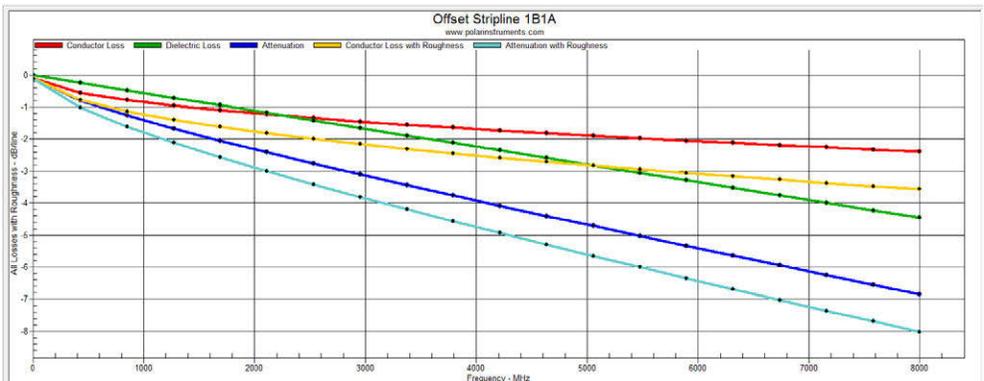


Figure 6.6: When roughness is taken into account, we have almost 8dB of loss.

In conclusion, when looking at high-frequency test requirements, you should always look “behind the specs” and ask the designer, “Does the speed refer to a single channel? Does the speed refer to a bit rate or a single frequency?” And when you know the answers to those questions, you and the designer can then investigate further as to whether the measurements required are those of simple lossless impedance or if additional information on transmission line insertion losses are also required.

This confirms that the answer to the question, “When is a 10GHz transmission line not a 10GHz transmission line?” is “It depends.”

The next chapter focuses on materials. The laminate materials used to fabricate PCBs are, for the most part, composites, and their composite parts often have different electrical properties. This is not necessarily a problem, but it is something to be aware of.

#### **Reference:**

1. Propagation Loss Test Methods Task Group (D-24b), May 2009 - IPC-TM-650 Test Methods Manual, Number 2.5.5.12 [ipc.org/4.0\\_Knowledge/4.1\\_Standards/test/2-5\\_2-5-5-12.pdf](http://ipc.org/4.0_Knowledge/4.1_Standards/test/2-5_2-5-5-12.pdf)



## CHAPTER 7

# **Regional Differences: A Voyage of Glass Reinforcement**

It is now time to slice into the materials themselves and explain why bulk  $\epsilon_r$  (relative permittivity) is not the same as local  $\epsilon_r$ .

Your experiences are coloured by the region you inhabit, and when you travel through your local region you probably encounter threads of different cultural experience. Even on a local level, a street may have an Italian or Chinese culture woven within the fabric of the city.

Threaded through printed circuit substrates are layers of glass cloth that provide dimensional stability and strength to the composite as a whole. And whilst discovering Italian or Chinese restaurants in a city is a pleasure, the discovery of a network of electrical variation in a substrate needs to be understood and catered to in the design. Back in the 1960s, could the originators of the material have ever conceived that this glass “insulator” would need to be considered from an electrical perspective other than its simple lack of conductivity?

A number of factors are converging, to the point where you do have to take the composite structure of base materials into account when you look at the high-speed performance of a PCB. The two primary drivers are the increase in data rates to the point where transmission line characteristics need to be understood, and the decrease in line width to a point where the traces are now small compared to the underlying bundles of fiberglass reinforcing the composite epoxy substrate.

Being composed of two quite differing materials, most woven glass substrates will exhibit quite different electrical characteristics on a “local” scale. Now that trace sizes are small compared with the fibre bundles,

the material characteristic “seen” by a signal can vary depending on the type of structure used and its physical dimensions. In FR-4 the epoxy may have an  $\epsilon_r$  of 3.6 while the glass  $\epsilon_r$  is typically more than 6. Figure 7.1 illustrates the cross-section of a typical controlled impedance structure in FR-4.

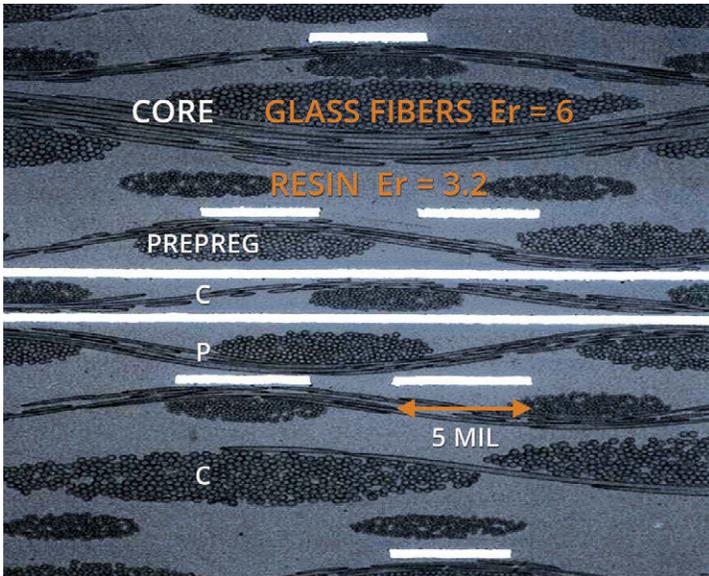
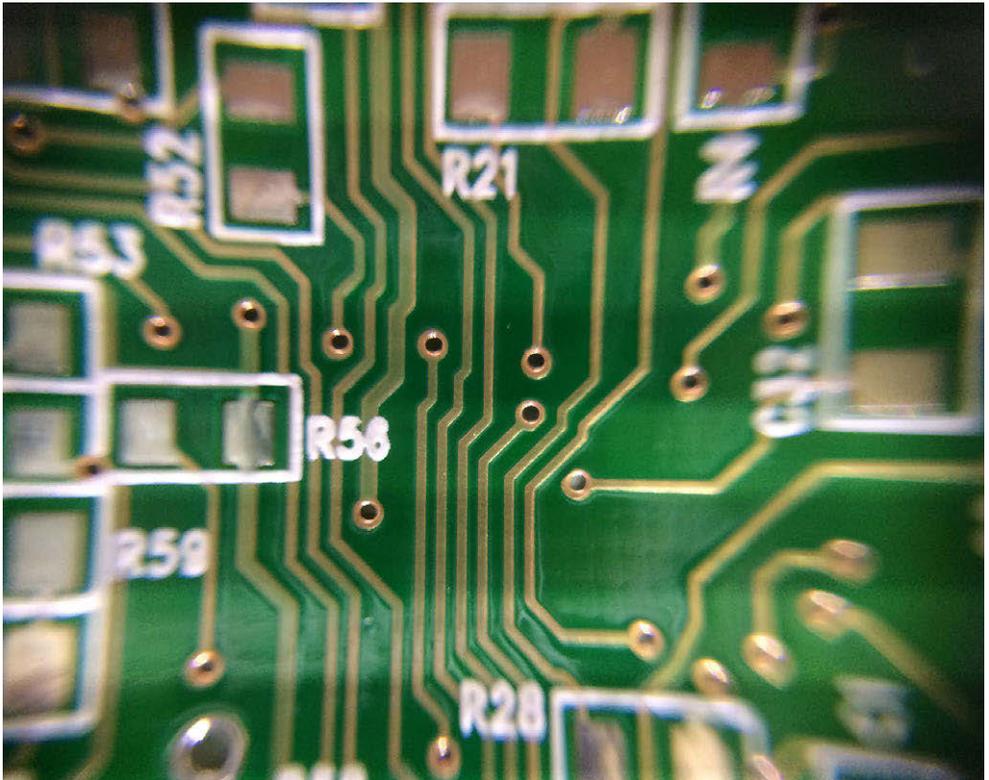


Figure 7.1: Cross-section of structure in glass-resin substrate.

So, the answer to “What is the  $\epsilon_r$  of that material?” is “It depends.” Is it the bulk  $\epsilon_r$ , as seen across a sample in a split post resonator, or the actual  $\epsilon_r$  seen by the signal as it transits along a trace? Striplines will have fields propagating to both adjacent planes, but coplanar structures will have fields that extend to the sides of the trace. A coplanar structure may “see” far less glass than a stripline structure, and not because of any change in material, but because the shape and density of the field is travelling through more resin than glass. In addition to the structure type, when considering edge-coupled differential structures, more tightly coupled designs that have the pair closely spaced will have a more intense field between the lines, in a region which will likely be predominantly filled with resin, again reducing the effective dielectric constant of the structure for that particular scale and geometry.



None of this results from problems with the base material; they are simply effects that are inherent when the substrate is a composite made from materials having two or more quite differing electrical properties.

In microwave or power applications where the traces may be much larger to reduce skin effect, the size of the trace may be large compared with the underlying fibre bundles, and in this situation the structure may behave much more as if it is built on a homogenous base.

You may have read about fibre weave mitigation in other articles. This is simply a technique of either rotating the PCB substrate so the glass weave is no longer parallel with the traces, or routing critical traces at an angle of 11 degrees or so to keep traces from lining up with a fibre bundle or a resin-rich area. Some laminate suppliers are working hard on materials with a tighter weave to reduce this effect. Another possibility is the use of glass materials with a lower  $\epsilon_r$  to reduce the mismatch in electrical properties of the substrate.

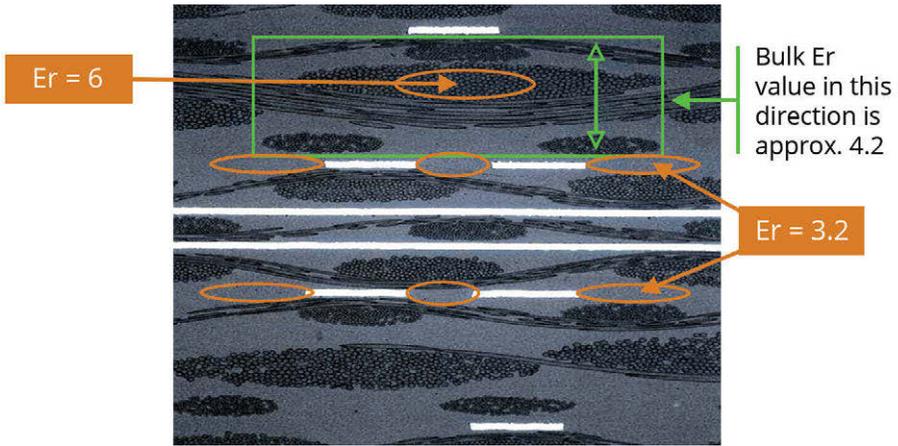
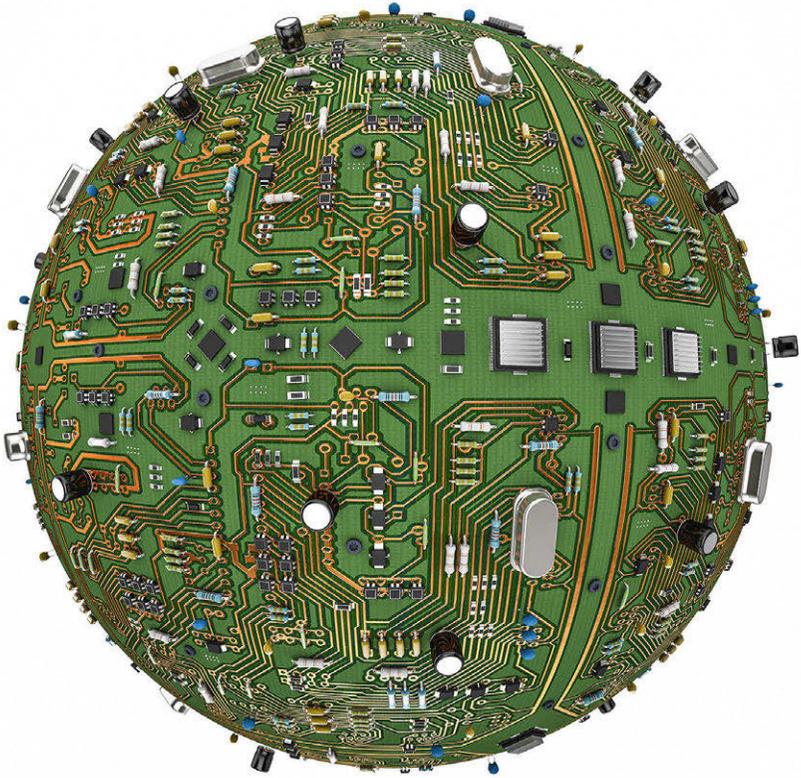


Figure 7.2: Cross-section showing bulk and local  $\epsilon_r$ .

Fortunately, impedance only varies as  $1/\sqrt{\epsilon_r}$ , so this variation is a second-order effect; however, when tolerances are tight it is important to know where sources of modelling error may creep in. When modelling any structure, it is worth looking at the range of  $\epsilon_r$  your signal may experience to ensure that the fabricator can hold the line width and dielectric separation tightly enough to allow for the possible variation of structure dependent  $\epsilon_r$ . Figure 7.2 illustrates bulk and local  $\epsilon_r$ . Modelling of the design space can ensure you choose structures and dimensions that are least sensitive to process changes.

In summary, remember that whilst engineering tools may lead you to think your designs work with ideal materials obeying the laws of physics to the  $n$ th degree, the actual materials you work with are, as with all engineered products, a compromise—trading off price, reliability and signal integrity. Being aware of the possible variations is the first step to ensure you provide enough headroom in your design to allow for normal process variations, thus avoiding any surprises in your final design.

Continuing with the theme of non-ideal materials and structures, the next chapter explains the benefits and limitations of using crosshatched ground returns in flex circuits.





## CHAPTER 8

# Crosshatching Compromise

In Chapter 7, we looked inside the material to the characteristics of its composite parts. Now, a look at intentional compromise.

Sometimes engineering results in some uncomfortable compromises; this is often the case with PCBs as the mathematical methods used by the modelling tools are based on “ideal” physical properties of materials rather than the actual physical materials in use. In previous chapters I have referred to this when considering the effects of glass woven reinforcement in base materials—the differing properties of the glass and the resin contribute to variations in electrical characteristics—given the scale of traces now in common use. The topic is well-known and much written about. However, this chapter discusses the subject of crosshatched ground planes (sometimes referred to as mesh ground planes) in transmission line structures.

This is another area where there is a necessary compromise between what the academics would treat as “ideal” and what has to be fabricated to make a practical board. I am referring to crosshatch (mesh) ground planes most often found on flex and flex-rigid PCBs. “It is not ideal,” say the academics. “Adding a crosshatch may widen the return path and may cause all sorts of problems at higher frequencies, possibly increasing crosstalk and EMC issues.”

However, first and foremost, flex circuits by definition should be mechanically flexible! If you try to construct a stripline with solid ground planes above and below the line (see Figure 8.1) the cross-section looks similar to an I-beam, a mechanically very stiff structure. So, whilst the signal integrity would arguably be enhanced, the board would fail mechanically in a very short time.

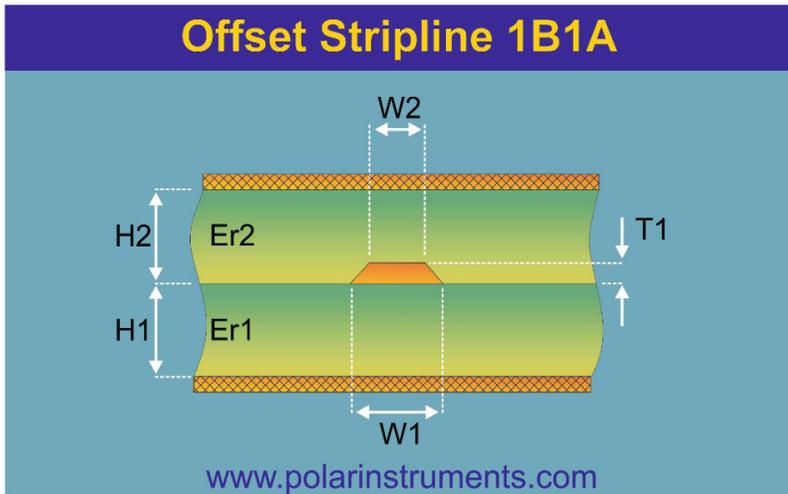


Figure 8.1: Stripline structure model using crosshatched planes.

To meet this challenge, it is possible, and commonplace, to use crosshatching to achieve a transmission line structure on a flex circuit and trade some signal integrity for durability. Fabricators, though, should consult with the EE responsible for the design to ensure that the hatch pattern is not so large to have significant impact at the upper frequencies. Just as for glass woven structures, the adoption of crosshatching means that the final structure is likely to have a broader tolerance from the modelled structure than a straightforward design using solid planes. However, it is always worth keeping in mind the words of George E.P. Box, professor emeritus of statistics at the University of Wisconsin, “Essentially, all models are wrong, but some are useful.” In the case of crosshatching, modelling should reduce the number of prototypes you need to turn to achieve the desired transmission line characteristics.

One other reason for using crosshatching on flex is that often the structures are very thin and in order to achieve the desired impedance, this can result in very narrow traces. Again, this means that impedance tolerance will broaden; the use of hatching will allow the fabricator to deploy wider traces and hence more predictable and tighter impedance tolerance.

As I write this, I am wondering whether coplanar structures could be used in place of crosshatch, and maybe some engineers already do that. The transmission line could then be constructed on a single layer, therefore overcoming the I-beam mechanical constraints of striplines and, to a

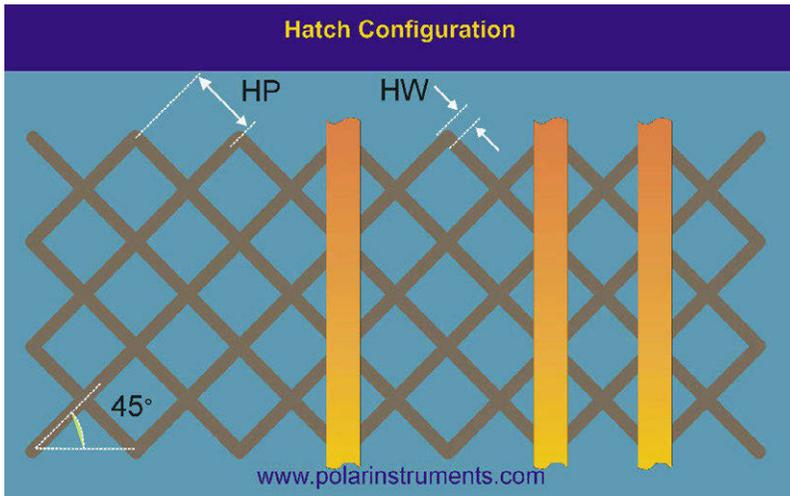


Figure 8. 2: Configuring crosshatch pitch and width.

lesser extent, microstrips. If any SI gurus are reading this, I would be delighted to hear your response.

I have, on occasion, also seen crosshatching used in rigid designs, again, to enable a designer to fabricate realistic line widths. But a more common practice is for the designer to reference the transmission line, not to the adjacent ground, but through an aperture in the adjacent ground, and then reference to a lower layer. This is subject to ensuring that no other high-speed lines traverse the aperture, thereby causing horrible transmission line discontinuities.

In summary, there is no right or wrong when deciding which route to take; the necessary adjustments need to be made to ensure the design is fit for purpose and that, like all engineering tasks, means loosening tolerances in some areas to allow you to tighten them in more critical ones. The task does become increasingly statistical when you are working to ensure that the design will remain in specification through the normal range of production variation. Design engineers should remain aware that crosshatch geometries should take into account the maximum harmonics in the design, and the possible impact on crosstalk and EMC.

Having considered the non-ideal effects of composite base materials and the effects of non-ideal ground return paths, we now move on to the next chapter to take a look at tolerance, specifically setting or interpreting realistic tolerances.



Figure 9.1: As I often note in my talks, a precision micrometer is of little use when measuring the dimensions of a jelly (jello).

## CHAPTER 9

# Tolerant of Tolerance?

Crosshatch, or mesh, as we discussed in the previous chapter, requires PCB specifiers to compromise their desire for tight specifications. This chapter investigates the concept of tolerance in greater depth.

Wouldn't life be great if everything was a perfect fit? There would be no need for tolerance. However, for that to be the case, everything would need to be ideal and without variation and, therefore, unfortunately (or maybe fortunately) we all deal with measurements and materials and situations that are not ideal and are compromised in one way or another.

Often the challenge with tolerance comes down to misunderstanding and the fact that we all now design with CAD tools that have levels of precision far in excess of the realisable parameters of the mechanical or electrical materials and measurement systems we deal with every day. Poor understanding of tolerance or being intolerant of tolerance can lead to disappointment.

As Aristotle is supposed to have said, "It is the mark of an instructed mind to rest satisfied with the degree of precision which the nature of the subject permits and not to seek exactness where only an approximation is possible." That translation itself is, of course, only an approximation and requires an appropriate degree of tolerance, but you get the idea.

Looking back a few decades, it is clear that the challenge in terms of tolerance and dimensioning shifted with the move from analog measurements to digital ones. Those of us in the industry for long enough can recall the move from analog voltmeters to digital, and from Vernier scale to digitally encoded micrometers and calipers. Electrically, there is the beginning of a second shift where high-speed digital systems blur back into the analog realm.

Digressing slightly, I recall a very analog moment when, as a naïve 11-year-old, I and a school friend decided to measure the current available from a wall socket—with an analog Avometer. (*Safety note: Not a wise move!*) The result was a large blue flash, melted meter cables and a visit from the local electricity authority as we had vaporised the main fuse in the supply box. Fortunately, we are both still here. Perhaps that’s why I ended up with a career in the electronics industry!



An early AVOMETER. Image credit: Creative Commons

Now, back to tolerance. In a supply chain, problems set in when tolerances are set incorrectly or when the tolerance specified is unachievable. The story dates back to the introduction of CAM and the ability to set hole tolerances far tighter than those achievable with the available drills or drilling machines. It is important that everyone in the supply chain understand what is achievable and what is not. The same is true for

electrical measurement. It also comes as no surprise that a long and complex supply chain also has a lot to take on board as each particular measurement can present individual challenges.

Take electrical measurements, for instance. I have described how the nature of electrical measurement changes as frequency increases. The same is true for tolerance. When measuring at low frequencies, current, voltage and resistance are all capable of being measured with a high degree of precision with many decimal places of accuracy and tolerance on measurements can be tight indeed. But as the frequency starts to creep up, it becomes harder to hold to such tight tolerances. At DC, tenths or hundredths of an ohm present little problem; at mid frequencies, say from 100MHz to 2GHz, measuring impedance presents more of a challenge. Perhaps a tolerance of 0.2 or 0.5 ohm is the best you can expect...and that depends on the impedance measured. Even the precision impedance air lines made traceable via NIST or NPL can present the user with a surprising amount of impedance uncertainty, limiting the achievable tolerance and absolute accuracy of measurement systems.

At even higher frequencies, resistance, voltage and current become even more tricky to measure. Instead, RF engineers resort to power measurement, in which the heating effect of the RF power is really the only way of measuring the gain or attenuation of a system, with voltages and currents being too elusive to measure. This is why you will see, as designers push high-speed digital to ever loftier transmission speeds, insertion loss,  $S_{21}$ , or differential insertion loss,  $SDD_{21}$ , is measured as a ratio of power into the line under test vs. power out. The difference between the power in and out will be the insertion loss.

Putting a tolerance on this type of measurement is tricky, as the measurement of the loss will depend as much on the design of the test pieces as on the metrology instrument. It is interesting to look at this from a distance because, to a casual observer, accurate low-frequency measurements need a good meter, but the probes can be quite simple and low-cost. As the frequency ramps up, shielding is often required and

then coaxial or transmission line probes. Additionally, the interconnect between the probe and the measurement system becomes a critical part of ensuring accuracy and repeatable measurements. At the highest frequencies, where ultimately a user may resort to a probe station, the probing system cost can be of a similar order to that of the measuring instrument. In fact, at high frequencies, all the parts of the measurement system need to be carefully crafted to ensure you can make accurate measurements within the desired tolerance; typically, the higher the frequency, the more the achievable tolerance widens out.

It is interesting to look at some VNA specifications regarding tolerance and accuracy. You will find that the measurement precision depends on a blend of factors, including the design of the test piece. For example, if a coupon is designed with a very high loss (almost complete signal attenuation) or very low loss (almost 100% transmission), it is hard to make an accurate measurement of loss per unit length. Samples, therefore, need to be designed with an appropriate loss depending on the base material used. Therefore, for low-loss materials the coupons may need to be longer (since loss is proportional to line length) than for a standard loss FR-4 material.

## **What increases your production tolerance?**

First—and, seemingly, one point that people miss—you need to allow for the tolerance of your measurement system. Some systems are very repeatable and sit well within their factory specifications, but the specifications are there for a reason. Do not assume that, because your measurements are very repeatable, they are more accurate than the published tolerance of the measurement system. Given that you have accepted this and you are working within the limits of your measurement system, let's take a look at controlled impedance traces and the possible offenders which may cause some of your products to fall outside—or close to—their permitted tolerance.

Cross-sections are important here. The primary drivers of impedance are dielectric separation and trace width. Trace thickness, along with dielectric constant, are second-order effects. It follows, then, that variation in line width may cause traces to vary in their measured impedance. Taking

several cross-sections can confirm if this is the case. As line width shrinks, it becomes more difficult to achieve a given level of tolerance. The same is true for dielectric separation, though this sometimes a surprise to designers. The board thickness does vary in different parts of the PCB—copper density is a key driver of this—and it is essential to ensure the copper density is well balanced to ensure there aren't excessive variations of height and therefore dielectric separation. Local variation of dielectric constant can also have an effect; witness the many white papers on fibre weave mitigation. However, low-twist fibres and mechanically spread glass can help with this issue, and perhaps in the future, the advances in glass design will reduce the need to deal with fibre weave variations in  $\epsilon_r$ .

It is interesting that spread glass is one of those rare win-win coincidences as it was originally developed to ease controlled-depth laser drilling, the resin being far easier to ablate than the glass. A side effect of the improved cloth is reduced regional variation in  $\epsilon_r$ . There is a third win here which no one saw coming: At very high (GHz) frequencies, the periodic variation in  $\epsilon_r$  caused by weave mitigation can cause high frequency variation in the insertion loss characteristics. This can almost be eliminated by the use of spread glass. But that's for another chapter.

In summary, when specifying any measurement, you should ensure that the design authority or supply chain procurement management specifies realistically. That means measuring within the limits of measurement capability of the available measurement systems and recognising that, in some cases, an appropriate sample measurement test vehicle (coupon or sample material) is an important part of the measurement system.

Finally, the key to keeping tolerance as tight as economically possible is an understanding of the materials and processes that are the key drivers of the property you are measuring.

And if you are still wondering if the Avometer survived its traumatic measurement experience, well, yes, it did.

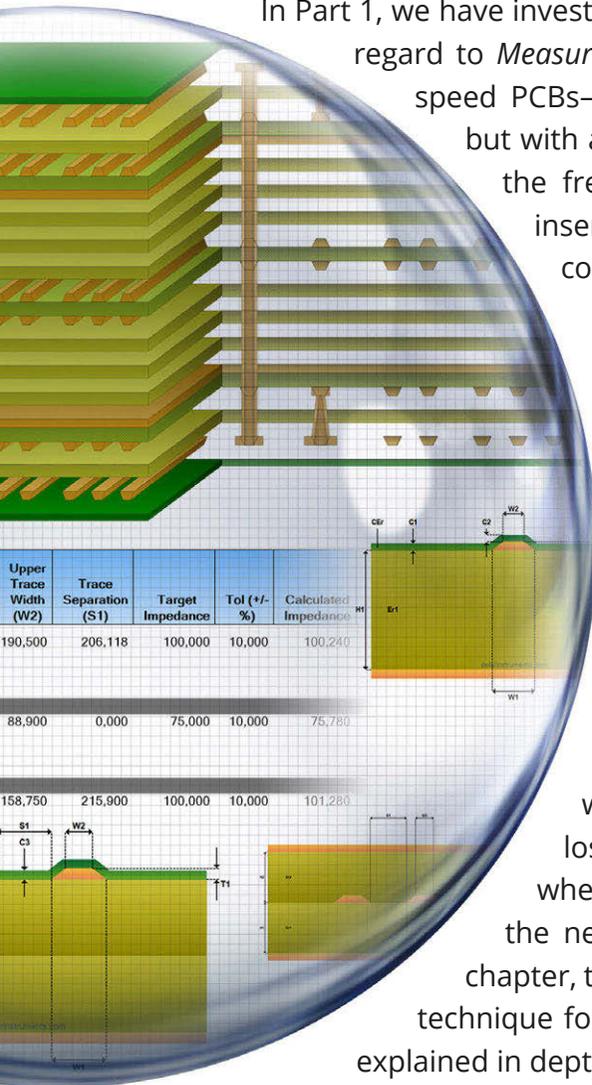
**Reference:**

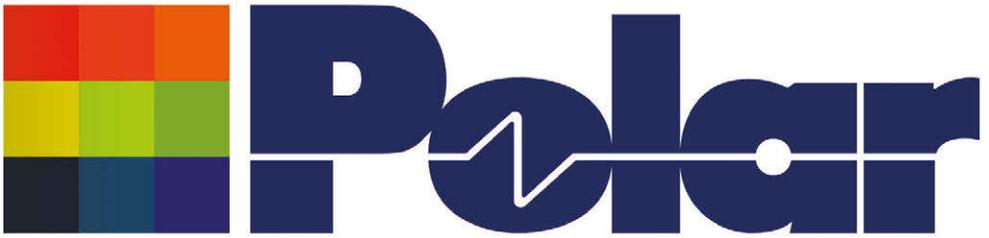
"A Designer's Guide to PCB Tolerancing," Polar Instruments Application Note AP521

# Summary

In Part 1, we have investigated some of the challenges with regard to *Measuring, Modelling, and Specifying* high-speed PCBs—primarily in the low GHz region, but with a few hints as to what to expect as the frequencies push into levels where insertion loss becomes the primary consideration.

In Part 2, we take a more extensive look at considerations for multi-gigahertz designs and note how the primary material and geometry drivers for insertion loss are very different from those that impact lower-frequency PCBs in the lossless impedance range. Last but not least, the penultimate chapter in Part 2, *Incident, Instantaneous, Impedance*, will study the twilight zone between lossless and insertion loss regions where fine lines have resulted in the need to consider DC losses. In this chapter, the launch point extrapolation (LPE) technique for impedance measurement will be explained in depth.





## About Polar Instruments

Polar Instruments specialises in designing EDA and measurement tools which simplify the design, fabrication, testing and specification of high-speed printed circuit boards (PCBs).

Polar's innovative product line includes the industry standard Controlled Impedance Test System (CITS), which provides the global PCB industry with an easy-to-use test system for high-speed digital and RF boards, as well as class-leading tools for fast and accurate design and testing of impedance and insertion loss controlled PCBs. Polar Speedstack is the layer stack-up design and documentation tool of choice for many designers, fabricators and PCB technologists.

Established in 1976, Polar Instruments now has operations and long-term channel partners in the United States, the United Kingdom, Europe and Asia Pacific.

Edge-Coupled Coated Microstrip 2

CEr C1 C2 S1 W2 T1

H2 Er2  
H1 Er1

www

Graph Results

Lossless Calculation

Angle: -45.43°  
Point 1: Left Button | Point 2: Right Button | Shift: Constrain 45° & 90°

Mouse [ 33471.95, 7652.759 ]  
Zoom [ 881.4 % ]  
Rotation [ 0.0 ° ]  
Units [ micron ]  
Coupon Surface Area [ 3233.32 mm² ]

**Polar**<sup>®</sup>

**Design, test and professional  
stackup documentation tools  
for high speed impedance and  
insertion loss controlled PCBs.**

[polarinstruments.com](http://polarinstruments.com)



## European Institute *for the* PCB Community

Linking PCB design and fabrication professionals  
with OEMs and suppliers through technical  
networking events and conferences.

[eipc.org](http://eipc.org)