

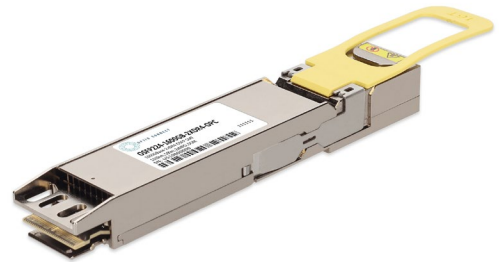


OSFP224-1600GB-2XDR4-OPC

MSA and TAA 1.6T 2xDR4 PAM4 OSFP224 Transceiver (SMF, 1310nm, 500m, 2xMPO, DOM, CMIS 5.0)

Features:

- OSFP224 Package
- Dual MPO-12 APC Optical Receptacle Connector
- 113GBaud EML LD
- 8x106.25GBaud PAM4 Electrical Interface
- Up to 500m Transmission on Single-Mode Fiber
- Power Consumption: 30W
- 3.3V Power Supply
- Hot-Pluggable
- Operating Temperature: 0°C to 70°C
- RoHS Compliant and Lead-Free



Applications:

- 16x100GBase Ethernet
- 2x800GBase Ethernet

Product Description

This MSA compliant OSFP224 transceiver provides 1600GBase-2xDR4 throughput up to 500m over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xMPO connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



Rev. 092925

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Tstg	-40		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Operating Relative Humidity	RH	5		85	%	
Supply Voltage	Vcc	-0.5	3.3	3.6	V	
Receiver Damage Threshold Per Lane		5			dBm	
Data Rate Per Lane	SR	106.25 ± 50ppm			GBd	
Modulation Format		PAM4				

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Supply Current	Icc		8.2		A	
Power Dissipation	P		27		W	
Transmitter						
Differential Pk-Pk Input Voltage	VIN			900	mV	
Differential Input Impedance	ZIN		100		Ω	
Transmitter Transition Time				8	ps	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λ	1304.5	1311	1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Optical Modulation Amplitude (OMA) Per Lane	OMAAouter	0.8		4.2	dBm	1
		1.2+Max. (TECQ,TDECQ)		4.2	dBm	2
Transmitter and Dispersion Eye Closure for PAM4 Per Lane	TDECQ			3.4	dB	
Over/Under-Shoot				22	%	
RIN _{21.4} OMA	RIN _{21.4} OMA			-139	dB/Hz	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of Off Transmitter Per Lane				-15	dBm	
Average Launch Power	Pavg	-3.3		4	dBm	
Receiver						
Center Wavelength	λ_C	1304.5	131	1317.5	nm	
Damage Threshold	PDamage	5			dBm	
Average Receiver Power Per Lane	PIN	-5.8		4	dBm	
Receiver Power Per Lane (OMA)	Overload			4.2	dBm	
Receiver Sensitivity (OMAAouter) Per Lane	SEN			-3.4	dBm	3
				-4.3+TECQ	dBm	4
Receiver Reflectance				-26	dB	
Differential Pk-Pk Input Voltage	VIN			TBD	mV	
Differential Input Impedance	ZIN		100		Ω	

Notes:

1. Output is coupled into a 9/125 μ m SMF.
2. Minimum average optical power measured at BER less than $1E^{-12}$. The measure pattern is PRBS $2^{31}-1$.

Control and Status I/O Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
MgmtInitDuration	Max. MgmtInitDuration			2000	ms	1
ResetL Assert Time	t_reset_init	10			μs	2
IntL Assert Time	ton_IntL			200	ms	3
IntL De-Assert Time	toff_IntL			500	μs	4
Rx_LOS Assert Time	ton_los			100	ms	5
Flag Assert Time	ton_flag			200	ms	6
Mask Assert Time	ton_mask			100	ms	7
Mask De-Assert Time	toff_mask			100	ms	8

Notes:

1. Time from power on, hot plug, or rising edge of reset until completion of the MgmtInit State.
2. Minimum pulse time on the ResetL signal to initiate a module reset.
3. Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
4. Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes de-assert times for Rx_LOS, Tx_Fault, and other flag bits.
5. Time from Rx_LOS state to Rx_LOS bit is set (value=1b), and the IntL is asserted.
6. Time from occurrence of condition triggering flag to associated flag bit is set (value=1b), and the IntL is asserted.
7. Time from mask bit is set (value=1b) until the associated IntL assertion is inhibited.
8. Time from mask bit is cleared (value=0b) until the associated IntL operation resumes.

Surge Current Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Module Power Supply Voltage Including Ripple, Droop, and Noise Below 100kHz	Vcc_Module	3.135	3.3	3.465	V	
Host Power Supply Voltage Including Ripple, Droop, and Noise Below 100kHz	Vcc_Host	3.135	3.3	3.465	V	
Module Power Supply Noise Tolerance 10Hz to 10MHz (Peak-to-Peak) Voltage Drop Across Mated Connector (Vcc_Host – Vcc_Module)	Vcc_drop			66	mV	
Total Current for Vcc Pins	Icc_module			10	A	1
Host RMS Noise Output 10Hz to 10MHz	e N_Host			25	mV	
Module RMS Noise Output 10Hz to 10MHz	e N_Mod			15	mV	
Module In-Rush to Instantaneous Peak Duration	T_ip			50	μs	
Module In-Rush to Initialization Time	T_init			500	ms	
In-Rush and Discharge Current	I_didt			100	mA/μs	2
High-Power Mode to Low-Power Mode Transition Time From Assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	μs	

Notes:

- Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure that the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.
- The specified in-rush and discharge current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high-power, and high-power to low-power.

Pin Descriptions

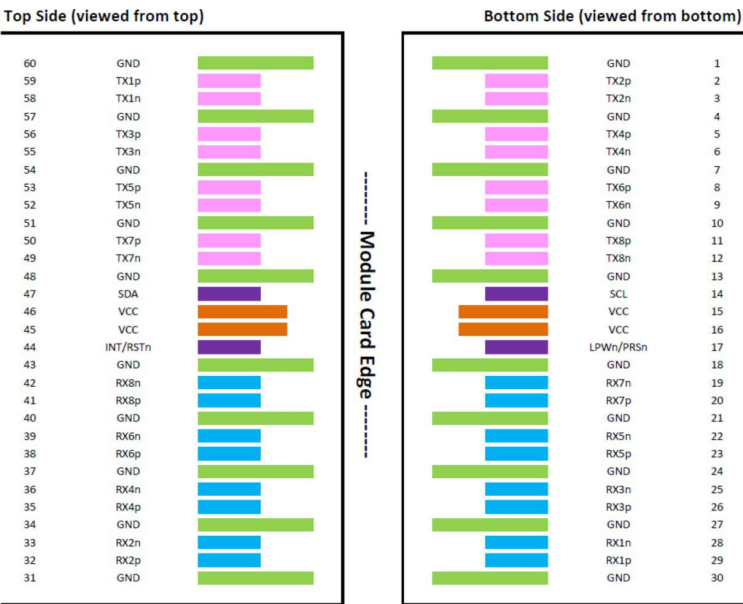
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2+	Transmitter Non-Inverted Data.	3	
3	CML-I	Tx2-	Transmitter Inverted Data.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4+	Transmitter Non-Inverted Data.	3	
6	CML-I	Tx4-	Transmitter Inverted Data.	3	
7		GND	Module Ground.	1	1
8	CML-I	Tx6+	Transmitter Non-Inverted Data.	3	
9	CML-I	Tx6-	Transmitter Inverted Data.	3	
10		GND	Module Ground.	1	1
11	CML-I	Tx8+	Transmitter Non-Inverted Data.	3	
12	CML-I	Tx8-	Transmitter Inverted Data.	3	
13		GND	Module Ground.	1	1
14	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	3	2
15		Vcc	+3.3V Power Supply.	2	
16		Vcc	+3.3V Power Supply.	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	3	3
18		GND	Module Ground.	1	1
19	CML-O	Rx7-	Receiver Inverted Data.	3	
20	CML-O	Rx7+	Receiver Non-Inverted Data.	3	
21		GND	Module Ground.	1	1
22	CML-O	Rx5-	Receiver Inverted Data.	3	
23	CML-O	Rx5+	Receiver Non-Inverted Data.	3	
24		GND	Module Ground.	1	1
25	CML-O	Rx3-	Receiver Inverted Data.	3	
26	CML-O	Rx3+	Receiver Non-Inverted Data.	3	
27		GND	Module Ground.	1	1
28	CML-O	Rx1-	Receiver Inverted Data.	3	
29	CML-O	Rx1+	Receiver Non-Inverted Data.	3	
30		GND	Module Ground.	1	1
31		GND	Module Ground.	1	1
32	CML-O	Rx2+	Receiver Non-Inverted Data.	3	
33	CML-O	Rx2-	Receiver Inverted Data.	3	
34		GND	Module Ground.	1	1
35	CML-O	Rx4+	Receiver Non-Inverted Data.	3	

36	CML-O	Rx4-	Receiver Inverted Data.	3	
37		GND	Module Ground.	1	1
38	CML-O	Rx6+	Receiver Non-Inverted Data.	3	
39	CML-O	Rx6-	Receiver Inverted Data.	3	
40		GND	Module Ground.	1	1
41	CML-O	Rx8+	Receiver Non-Inverted Data.	3	
42	CML-O	Rx8-	Receiver Inverted Data.	3	
43		GND	Module Ground.	1	1
44	Multi-Level	INT/RSTn	Module Input/Module Reset.	3	3
45		Vcc	+3.3V Power Supply.	2	
46		Vcc	+3.3V Power Supply.	2	
47	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	3	2
48		GND	Module Ground.	1	1
49	CML-I	Tx7-	Transmitter Inverted Data.	3	
50	CML-I	Tx7+	Transmitter Non-Inverted Data.	3	
51		GND	Module Ground.	1	1
52	CML-I	Tx5-	Transmitter Inverted Data.	3	
53	CML-I	Tx5+	Transmitter Non-Inverted Data.	3	
54		GND	Module Ground.	1	1
55	CML-I	Tx3-	Transmitter Inverted Data.	3	
56	CML-I	Tx3+	Transmitter Non-Inverted Data.	3	
57		GND	Module Ground.	1	1
58	CML-I	Tx1-	Transmitter Inverted Data.	3	
59	CML-I	Tx1+	Transmitter Non-Inverted Data.	3	
60		GND	Module Ground.	1	1

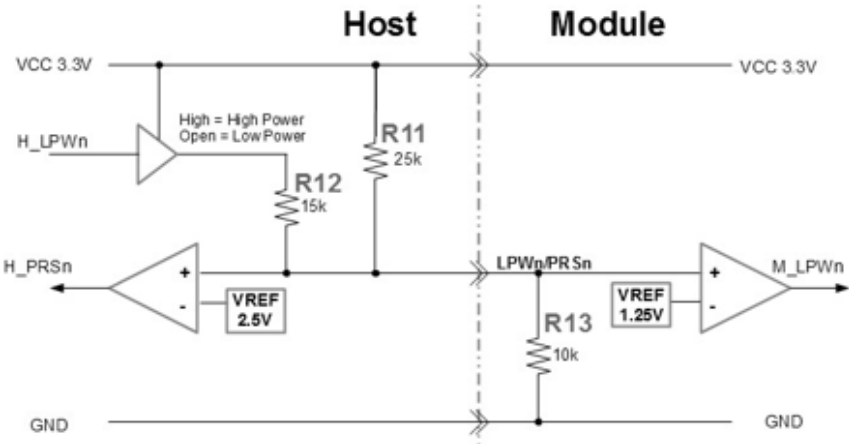
Notes:

1. OSFP uses common ground (GND) for all signals and supply (power). All are common within the OSFP module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. SCL and SDA are 2-wire serial interfaces between the host and the module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal, and SDA is defined as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1kΩ to 4.7kΩ depending on the capacitive load.
3. LPWn/PRSn is a dual-function signal that allows the host to signal low-power mode and allows the module to indicate that the module is present. The circuit shown in the “LPWn/PRSn Circuit” enables multi-level signaling to provide direct signal control in both directions. Low-power mode is an active-low signal on the host which gets converted to an active-low signal on the module. “Module Present” is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

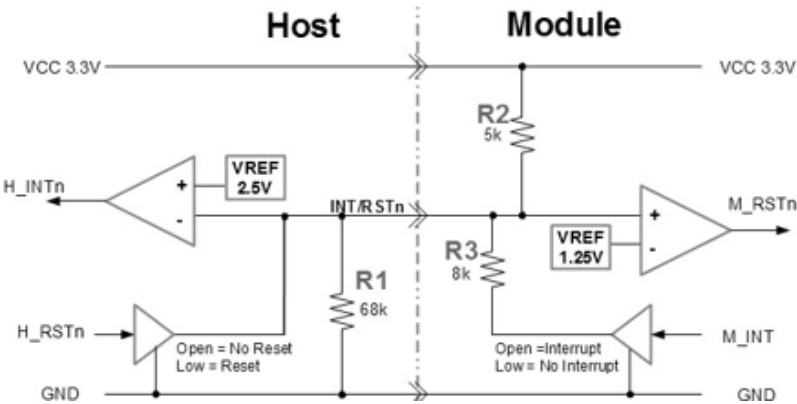
Host Board Connector



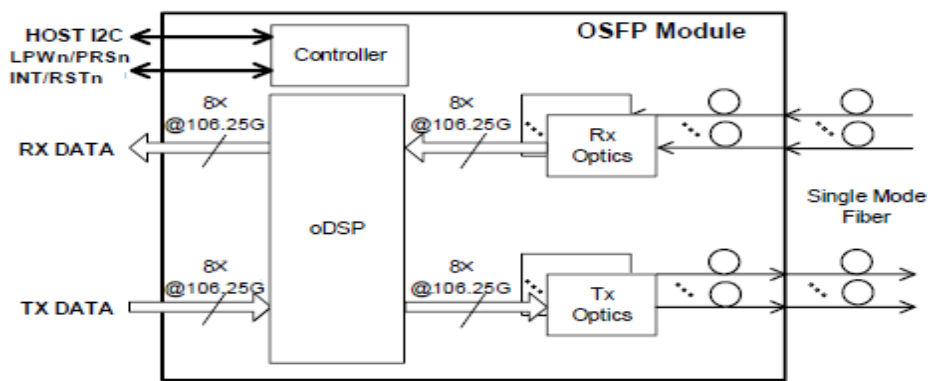
LPWn/PRSn Circuit



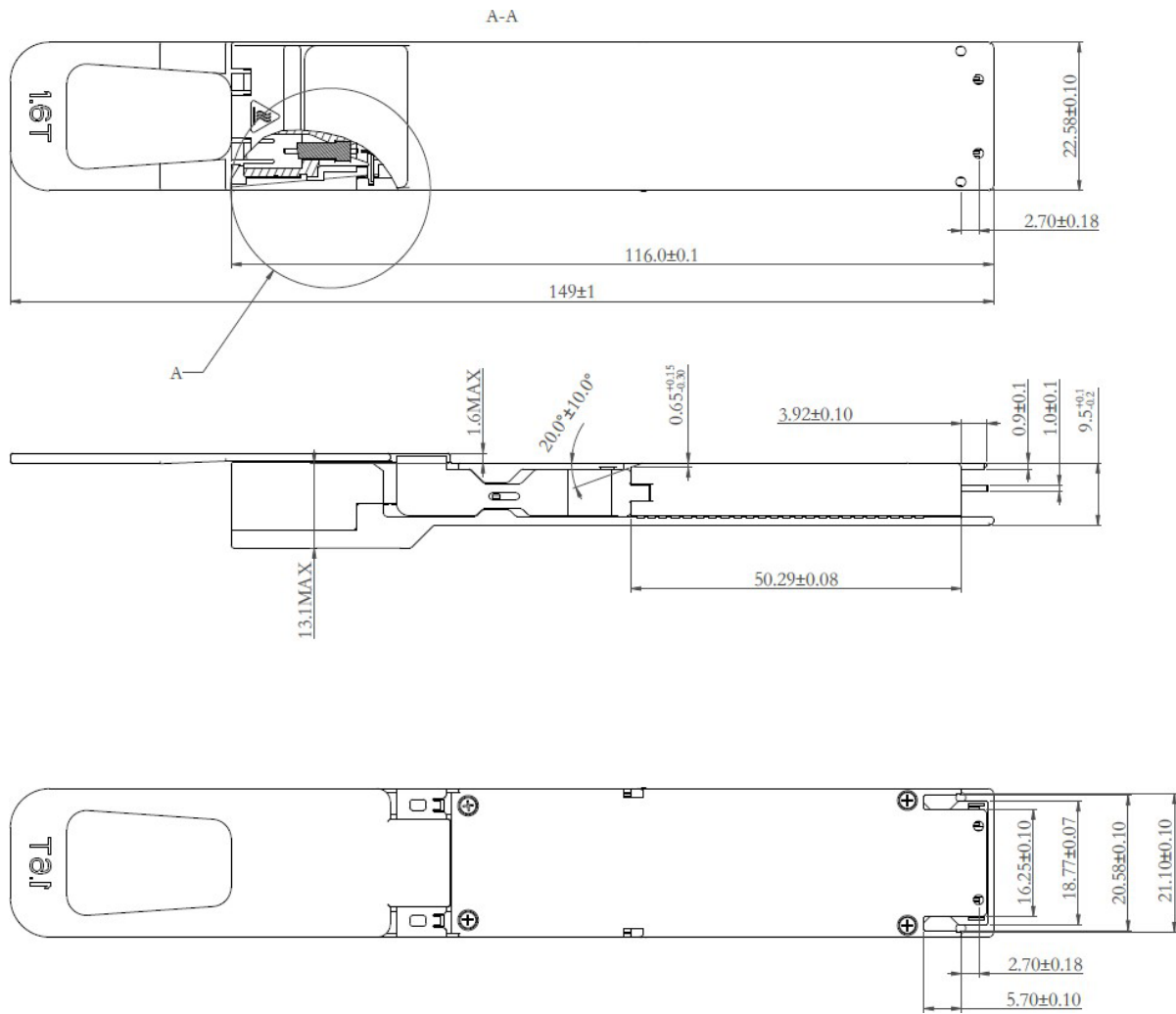
INT/RSTn Circuit



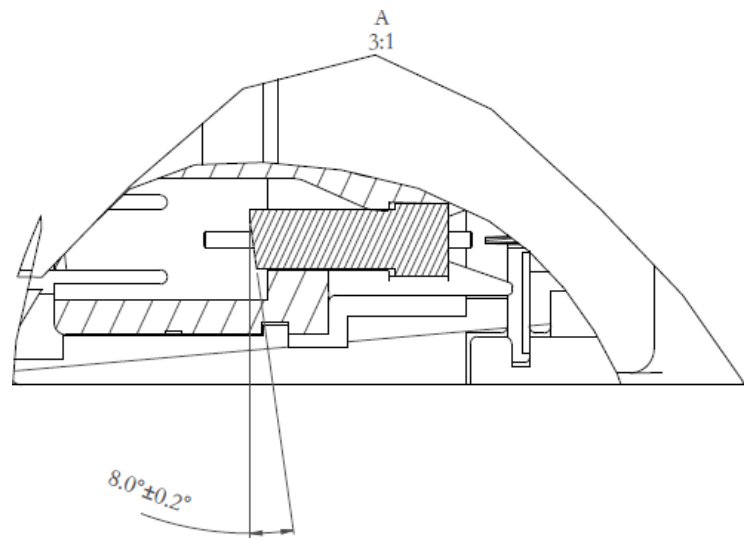
Block Diagram



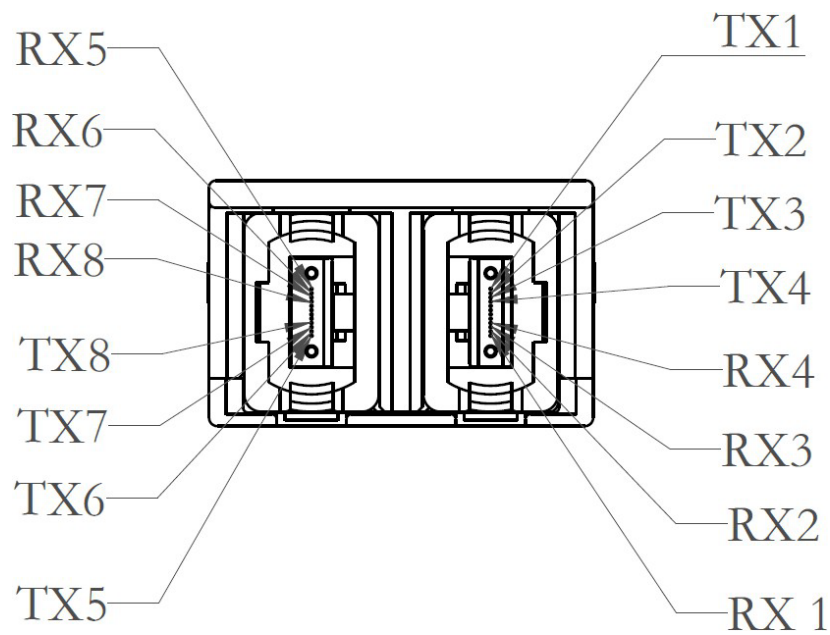
Mechanical Specifications



Enlarged View of Detail A



Enlarged View of Detail B



OptioConnect

Innovation for the Future of High-Speed Networking

Who We Are

OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

What We Do

At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

Smarter Networks by Design

Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

Our Team

Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

Our Mission

To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

Let's Connect

Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.

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