21037 AD2

The implementation of the OpenScope, a 1 MHz PIC32 MZ based IoT WiFi Oscilloscope, and more
Who am I?

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Class Objectives

- How to use the OpenScope and its limitations.
- Hardware design overview of each instrument.
- Interleave ADCs to obtain a higher sampling rate.
- Use software calibration to reduce component cost and improve accuracy.
Class Objectives Continued

- Use DMA to off-load the CPU and improve performance.
- Trigger various Instruments
- Implement R2R Ladder DAC to create waveform generator.
- Communicate to OpenScope via WiFi HTTP or USB COM JSON interface.
- How to build OpenScope source.
Open Scope Agenda

- Open Scope Waveforms Live Demonstration
- Architecture
- Resource Allocation
- DC Outputs
- Precision Analysis
- Analog Inputs
- DMA Parallel Processing
- ADC Interleaving
- Logic Analyzer (LA)
- Scope Triggering
- Analog Waveform Generator (AWG)
- Priority and Stalling Consequences
- USB/Serial, UART Interface
- Open Scope Text Based Protocol
- Building the Sources
OpenScope Features

$89.00

- 2 Oscilloscope channels with 12 bits at 2MHz bandwidth and 6.25 MS/s max sampling rate
- 1 function generator - 1MHz bandwidth @ 10 MS/s update rate
- 10 Logic Analyzer inputs or user programmable pins @ 10 MS/s update rate
- 2 User programmable power supplies supplying up to 50mA and ± 4V power
- WiFi or USB interface
- Browser-based WaveForms Live multi-instrument software
OpenScope Layout

- USB->UART
- MRF24WG WiFi Radio
- PIC32MZ
- AWG R2R Ladder
- Gain Select
- MCP6H82 / 91 AWG DC output OpAmp
DEMO LC TANK
PIC® MCU based LC Tank
LC Tank Demo Board

5.7x Gain
2017

MASTERs
Conference

Architecture
User Interface Communications

- **OpenScope HTTP Server**
  - Post Body: JSON Text Scope Commands

- **Digilent Agent HTTP Server**
  - Ethernet
  - WiFi
  - Local/Remote Access
  - USB
  - FTDI USB/Serial

- **Common JSON Command Parser**
  - Hardware Control

- **OpenScope**
  - WiFi
  - http://<OS IP>:80
  - http://<PC IP>:42135
  - http://localhost:42135

- **COM/UART**
  - JSON Text Scope Commands

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Major Components

- **Hardware**
  - PIC32MZ, MRF24 WiFi Radio, USB/Serial, uSD, Analog Circuits, Flywires

- **Firmware**
  - Instrument operation, Calibration, Communication, WiFi, Storage

- **Waveformslive (WFL)**
  - Browser Based UI (local and remote internet)
  - Native iOS and Android Apps

- **Digilent Agent (DA)**
  - USB/Serial Communication, Setup, Local/Remote Internet Connectivity
Hardware Block Diagram

**PIC32 Resource Usage Summary Table**

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**Analog Inputs**

- +/-20V
- 2 Channels
- 1 MHz BW

**DC Outputs**

- 2 Channels
- -4V to +4V

**PWM Outputs**

- 2 Channels
- MUX
- 2 Ch

**DAC Outputs**

- 2 Ch
- 5 DC Outputs
- 2 Offsets

**DAC Output Generator**

- 2 Ch
- MCP6H82
- 5 PWM

**PSD Output**

- 10 LA
- 10 MS/s

**EXT Trigger**

- Button
- Reset Button

**Logic Analyzer**

- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

**Triggering**

- 2 GPIO
- 1 INT

**USB via UART**

- 1 UART
- 2 DMAs

**uSD**

- 1 SPI

**WiFi**

- 1 SPI / INT

**PIC32MZ2048EFG124**

- MUX Select:
  - 4 GPIO
- Channel 1 / 2:
  - 2 OC/PWMs
  - 3 TMRs
  - 4 DMAs
  - 4 Ded. ADCs
- PGM Button
- Reset Button
- High Precision 3V Ref
- DC Generators:
  - 5 OC/PWMs
  - 2 TMRs
- 8 Feedback ADC
  - 2 DC
  - 1 AWG
  - 5 Supply/Ref
- AWG:
  - 1 TMR Shared
  - 1 DMA Shared
  - Port H
- Protocol I/O:
  - 1 SPI / UART
  - 1 I2C
  - 5 GPIO
  - 1 DMA
  - 2 OC/PWMs
  - 1 TMR
  - 2 INTs
- Logic Analyzer:
  - 10 GPIO
  - 1 TMR Shared
  - 1 DMA Shared
  - 1 INT
- Triggering:
  - 2 GPIO
  - 1 INT
- USB via UART:
  - 1 UART
  - 2 DMAs
- uSD:
  - 1 SPI
- WiFi:
  - 1 SPI / INT

**AWG**

- MCP6H91
- R2R Ladder

**Digital Filters**

- 1 of 6

**Digital Compare**

- 2 of 6

**Dedicated ADCs**

- 4 of 5

**Shared ADCs**

- 8 of 43

**Digital Compare**

- 2 of 6

**USB via UART**

- 1 UART
- 2 DMAs

**uSD**

- 1 SPI

**WiFi**

- 1 SPI / INT

**FTDI (USB for Serial COM)**

- Port E
- 10 LA

**EXT Trigger**

- Port F
Resource Allocation
Resource Allocation

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

USB:
- 1 SPI

WiFi:
- 1 SPI / INT

Port F

10 LA Inputs

Port E

10 MS/s

EXT Trigger

DC Generators:
- 5 OC/PWMs
- 2 TMRs

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

PIC32
Resource Usage Summary Table

PWM / OC | 9 of 9
---|---
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I2C | 1 of 5
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PIC32 Peripheral Resources

- PWM are used to drive offset voltages for the DCout, Analog In, and AWG. Also used for interleave ADC triggers.

- Timers are used to trigger ADCs, DMA transfers, PWMs, and Trigger delays

- DMA used to transfer ADC/AWG/LA and Serial Data without CPU utilization.
Resources

- **ADCs**
  - 4 Dedicated (Scope 1, 2), 8 Shared Calibration Feedback
- **ADC Digital Compares**
  - 2 ADC (Scope 1, 2 High/Low Triggers), 4 Spares
- **PWMs**
  - 3 Offset, 2 ADC Interleave, 2 DC, 2 User
- **Timers**
  - 2 ADC, 1 DC/OC, 1 Offset/OC, 1 AWG/LA, 1 Trigger, 1 protocol, 2 spare
Resource Continued

- **DMAs**
  - 2 UART, 4 ADC (Scope 1,2), 1 AWG / LA, 1 Protocol

- **UARTs**
  - 1 COM (Digilent Agent), 1 Protocol, 4 spares

- **SPI**
  - 1 MRF24WG WiFi Radio, 1 μSD, 1 protocol, 1 unavailable, 2 spares.

- **External Interrupts**
  - 1 MRF24WG WiFi Radio, 3 External Triggers, 1 Protocol
DC Outputs
DC Outputs

**PIC32MZ2048EFG124**

- **MUX Select:**
  - 4 GPIO
- **Channel 1/2:**
  - 2 OC/PWMs
  - 3 TMRs
  - 4 DMAs
  - 4 Ded. ADCs
- **Protocol I/O:**
  - 1 SPI / UART
  - 1 I2C
  - 5 GPIO
  - 1 DMA
  - 2 OC/PWMs
  - 1 TMR
  - 2 INTs
- **Logic Analyzer:**
  - 10 GPIO
  - 1 TMR Shared
  - 1 DMA Shared
  - 1 INT
- **DC Generators:**
  - 5 OC/PWMs
  - 2 TMRs
- **8 Feedback ADC:**
  - 2 DC
  - 1 AWG
  - 5 Supply/Ref
- **USB via UART:**
  - 1 UART
  - 2 DMAs
- **uSD:**
  - 1 SPI
- **WiFi:**
  - 1 SPI / INT

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**ANALOG INPUTS**

- +/-20V
- 2 Channels
- 1 MHz BW

**DC Outputs**

- 5 DC Outputs from PWMs
- 2 Channels
- -4V to +4V

**PWM / Op Amp**

- LMV116 / Op Amp
- TS3A5017 / MUX

**DC Generators**

- 5 OC/PWMs
- 2 TMRs

**PWM**

- AWG: MCP6H82 / LMV324IDT
- R2R Ladder
- 10 bit
- Port H

**Logic Analyzer**

- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

**AVG Output**

- AWG: MCP6H91
- EXT Trigger
- Button
- Reset Button

**Digital Compare**

- 2 of 6

**Digital Filters**

- 1 of 6

**USB**

- FTDI (USB for Serial COM)

**External Inputs**

- Port F
- Port E

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OpAmps 101 a Refresher

\[ V_{Oac} = \left( -\frac{R_{fb}}{R_{ac}} \right) \cdot V_{ac} \]
\[ V_{Opwm} = \left( -\frac{R_{fb}}{R_{pwm}} \right) \cdot V_{pwm} \]
\[ V_{Obias} = \left( -\frac{R_{fb}}{R_{bias}} \right) \cdot V_{bias} \]

\[ V_{O} = \left( -\frac{R_{fb}}{R_{ac}} \right) \cdot V_{ac} + \left( -\frac{R_{fb}}{R_{pwm}} \right) \cdot V_{pwm} + \left( -\frac{R_{fb}}{R_{bias}} \right) \cdot V_{bias} \]
OpAmp Gain and Offset Math

\[ V_O = \left(-\frac{R_{fb}}{R_{ac}}\right) \cdot (V_{ac} - V_{ref}) + \left(-\frac{R_{fb}}{R_{pwm}}\right) \cdot (V_{pwm} - V_{ref}) + \left(-\frac{R_{fb}}{R_{bias}}\right) \cdot (V_{bias} - V_{ref}) + V_{ref} \]

Let \( A = \left(-\frac{R_{fb}}{R_{ac}}\right) \); \( B = \left(-\frac{R_{fb}}{R_{pwm}}\right) \); \( C' = \left(-\frac{R_{fb}}{R_{bias}}\right) \)

\[ V_O = A \cdot V_{ac} + B \cdot V_{pwm} + C' \cdot V_{bias} - (A + B + C' - 1) \cdot V_{ref} \]

\[ V_O = \left(-\frac{R_{fb}}{R_{ac}}\right) \cdot V_{ac} + \left(-\frac{R_{fb}}{R_{pwm}}\right) \cdot V_{pwm} + \left(-\frac{R_{fb}}{R_{bias}}\right) \cdot V_{bias} \]
\[ + \left( \frac{R_{fb}}{R_{ac}}\right) \cdot V_{ref} + \left( \frac{R_{fb}}{R_{pwm}}\right) \cdot V_{ref} + \left( \frac{R_{fb}}{R_{bias}}\right) \cdot V_{ref} + V_{ref} \]

Let \( C = C' \cdot V_{bias} - (A + B + C' - 1) \cdot V_{ref} = \left(-\frac{R_{fb}}{R_{bias}}\right) \cdot (V_{bias} - V_{ref}) - (A + B - 1) \cdot V_{ref} \)

\[ V_O = A \cdot V_{ac} + B \cdot V_{pwm} + C \]
PWM, DC Outputs and Offsets

- Bias input PWM voltage of 1.75V to center PWM control range
- PWM, DC Outputs and Offsets
- 34Hz Cutoff
- ADC Feedback for Calibration
- Bias Noise Filter
- Reference Noise Filter
- Feedback Noise Filter
- OpAmp Ref voltage
- Summing Node
- DC Output

Bias

Gain is \(-12/3 = -4\)

PWM design range is 50 – 300 of 330
Or
0.5v to 3.0v with a voltage delta of 2.5V
2.5 * 4 = 10v dynamic range centered on zero

PWM runs at 303KHz
PWM Design Limits

- PWM has 330 unique values.
- The PWM output will be from 0 to Vcc (3.3v), so each PWM value corresponds to 10mV.
- The PWM internal clock runs at 100MHz, so the frequency of the PWM is $100\text{MHz}/330 = 303\text{KHz}$.
- All PWM analog design ranges are from 50 to 300 to allow for headroom calibration; center around 175.
PWM Usage and Considerations

- 5 PWMs provide DC outputs and offsets.
  - 2 DC output circuits
  - 3 offset circuits
    - 2 Analog-in offsets
    - 1 AWG offset
- There are at least 2 filters, one close to the MCU so DC is routed about the board, one near its final usage to filter out crosstalk noise
- There is a setup time of approx 30 - 100ms; The software uses 500ms, about 500 time constants
Most Circuits are described as Polynomials

- \( \mu V = A \cdot D_{adc} + B \cdot D_{pwm} + C \)
- DC Feedback
  - \( \mu V_{DC_{out}} = (595000000 \cdot D_{adc} - 409600000000 \cdot V_{Ref3.0}) / 241664 \)
- DC Output
  - \( \mu V_{DC_{out}} = -40,000 \cdot D_{pwm} + 7,000,000 \)
- Analog Input
  - \( \mu V_{in} = (13,183,593.75 / R_{1Sx}) \cdot D_{adc} + (154,338,032 / R_{2Sx}) \cdot D_{pwm} - (27,000,000,000 / R_{2Sx}) \)
- Waveform Generator (AWG)
  - \( \mu V_{awg} \approx -2987 \cdot D_{dac} - 11995 \cdot D_{pwm} + 3630161 \)
  - \( \mu V_{PWM\, Offset} = -11995 \cdot D_{pwm} + 2099125 \)
  - Table Lookup – Best Fit for \( D_{dac} \)
DC Feedback: $V = A \cdot D_{adc} - B$

\[
V_{adc} = \left(\frac{3}{4096}\right) \cdot D_{adc} = \frac{(R_{124})(R_{128})}{((R_{124})(R_{126}) + (R_{126})(R_{128}) + (R_{124})(R_{128}))} \cdot DC_{out} + V_{Ref3.0} \cdot \frac{(R_{126})(R_{128})}{((R_{124})(R_{126}) + (R_{126})(R_{128}) + (R_{124})(R_{128}))}
\]

\[
D_{adc} = \frac{4096}{3} V_{adc} = \frac{241664}{595} \cdot DC_{out} + \frac{81920}{119} \cdot V_{Ref3.0}
\]

OR

\[
\mu V_{DC_{out}} = \frac{595000000 \cdot D_{adc} - 409600000000 \cdot V_{Ref3.0}}{241664}
\]

For:

- $DC_{out} = -5; \ D_{adc} = 34; \ V_{adc} = 0.02521 V$;
- $DC_{out} = 0; \ D_{adc} = 2065; \ V_{adc} = 1.5126 V$;
- $DC_{out} = 5; \ D_{adc} = 4096; \ V_{adc} = 3.0 V$;
$\text{DC}_{\text{out}}: V = -A \cdot D_{\text{pwm}} + B$

$$\text{DC}_{\text{out}} = \frac{-R_{90}}{(R_{87}+R_{88}+R_{87})} \cdot V_{\text{CC3.3}} / 330 \cdot D_{\text{pwm}} + V_{\text{Ref1.5}} \cdot \frac{R_{90}}{(R_{87}+R_{88}+R_{87})} + (V_{\text{Ref1.5}} - V_{\text{Ref3.0}}) \cdot \frac{R_{90}}{R_{91}+R_{92}} + V_{\text{Ref1.5}}$$

$$\text{DC}_{\text{out}} = -0.04 \cdot D_{\text{pwm}} + 7$$

OR

$$\mu V_{\text{DC}_{\text{out}}} = -40000 \cdot D_{\text{pwm}} + 7000000$$

$A = 40000$; $B = 7000000$

For:

- $D_{\text{pwm}} = 50$; $\text{DC}_{\text{out}} = 5.0V$
- $D_{\text{pwm}} = 175$; $\text{DC}_{\text{out}} = 0.0V$
- $D_{\text{pwm}} = 300$; $\text{DC}_{\text{out}} = -5.0V$
DC_{out} Calibration

\[ \mu VDC_{1out} = -A \cdot D_{1pwm} + B \]
\[ -\mu VDC_{2out} = A \cdot D_{2pwm} - B \]

\[ \mu VDC_{1out} - \mu VDC_{2out} = A \cdot (D_{2pwm} - D_{1pwm}) \]

A = \frac{\mu VDC_{1out} - \mu VDC_{2out}}{D_{2pwm} - D_{1pwm}}
B = \mu VDC_{1out} + A \cdot D_{1pwm}

A \approx 40000
B \approx 7000000
Precision Analysis
**Precision Analysis**

**PIC32MZ2048EFG124**

- **MUX Select:**
  - 4 GPIO
- **Channel 1 / 2:**
  - 2 OC/PWMs
  - 3 TMRs
  - 4 DMAs
  - 4 Ded. ADCs
- **Protocol I/O:**
  - 1 SPI / UART
  - 1 I2C
  - 5 GPIO
  - 1 DMA
  - 2 OC/PWMs
  - 1 TMR
  - 2 INTs
- **Logic Analyzer:**
  - 10 GPIO
  - 1 TMR Shared
  - 1 DMA Shared
  - 1 INT
- **DC Generators:**
  - 5 OC/PWMs
  - 2 TMRs
- **Triggering:**
  - 2 GPIO
  - 1 INT
- **USB via UART:**
  - 1 UART
  - 2 DMAs
- **uSD:**
  - 1 SPI
- **WiFi:**
  - 1 SPI / INT

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**Analog Inputs**

- +/-20V
  - 2 Channels
  - 1 MHz BW

**DC Outputs**

- 5 DC Outputs from PWMs
  - 2 Ch
  - 2 Offsets
  - +/-20V
  - 2 Channels
  - -4V to +4V

**AWG Outputs**

- 10 bit
  - Port H

**Logic Analyzer:**

- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

**EXT Trigger**

- FTDI (USB for Serial COM)
- uSD
- MRF24 WiFi

**ICs:**

- LMV116 / Op Amp TS3A5017 / MUX
- MCP6H82 / LMV324IDT
- LM4040A1M3
- PIC32MZ2048EFG124
- MCP6H91
Where Precision and Accuracy is Needed

- The 3 volt reference is the most critical component.
- The MZ ADC must be accurate, the 3 volt reference must go directly and cleanly into the MZ ADC reference.
- Feedback circuits used to calibrate must be accurate and assumed to be true.
Where is Precision Needed

Must assume feedback resistors are accurate

We can measure these voltages

Must assume 3v reference is accurate

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Where Accuracy is Not Needed

- Resistor only need to be 5% and Capacitors 20%.
  - We use 1% Resistors and 10% Capacitors
- Voltages, including distributed voltage references are all measured and accounted for mathematically.
- Opamps only need to behave linearly.
OpAmp Considerations

- Use inexpensive OpAmps <50¢
  - Common Mode Input Considerations
    - High input capacitance.
    - Not rail to rail, often as low as Vcc – 1.3v.
    - High input bias currents.
    - Non-linear input bias currents.
    - Non-linear as you approach input limits.
  - Output Considerations
    - Not rail to rail outputs.
    - Headroom drop-off; $V_{out} = Vcc - HR(mA_{out})$. 
OpAmp Usage

- **Use inverting mode for AC signals**
  - Common Mode Input
    - Fixed operating input voltage, the reference voltage.
    - Constant input bias current.
    - Will not approach input limits.
    - Operate at ideal voltage, at or near Vcc /2
      - Most linear operation
  - **May use non-inverting mode for DC**
    - Select an OpAmp with good Headroom/rail-to-rail characteristics, vs bandwidth: LMV324IDT.
Analog Inputs
Analog Inputs

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</tr>
<tr>
<td>1 of 6</td>
<td>1 of 6</td>
</tr>
</tbody>
</table>

**Analog Inputs**

- **5 DC Outputs from PWMs**
  - 5 DC Outputs
  - from PWMs
  - +/20V
  - 2 Channels
  - 1 MHz BW

- **2 Offsets**
  - +/20V
  - 2 Channels
  - -4V to +4V

- **DC Generators**
  - 5 DC Outputs
  - from PWMs
  - -3V
  - 2 Channels

- **10 LA Inputs**
  - 10 MS/s

- **EXT Trigger**
  - Button
  - PGM Button
  - Reset Button

- **High Precision 3V Ref**

- **MCP6H82 / LMV324IDT**

- **R2R Ladder**

- **MCP6H91**

- **LMV116 / Op Amp**
  - TS3A5017 / MUX
  - 1
  - 4
  - 8
  - 40

- **PIC32MZ2048EFG124**
  - MUX Select:
    - 4 GPIO

- **Channel 1 / 2:**
  - 2 OC/PWMs
  - 3 TMRs
  - 4 DMAs
  - 4 Ded. ADCs

- **DC Generators:**
  - 5 OC/PWMs
  - 2 TMRs

- **8 Feedback ADC:**
  - 2 DC
  - 1 AWG
  - 5 Supply/Ref

- **AWG:**
  - 10 bit
  - Port H

- **PWM / OC**
  - 9 of 9

- **Timers**
  - 7 of 9

- **INTs**
  - 5 of 5

- **SPI**
  - 3 of 6

- **UART**
  - 2 of 6

- **I2C**
  - 1 of 5

- **DMAs**
  - 9 of 8

- **Dedicated ADCs**
  - 4 of 5

- **Shared ADCs**
  - 8 of 43

- **Digital Compare**
  - 2 of 6

- **Digital Filters**
  - 1 of 6

- **AWG: WiFi**
  - MRF24

- **Protocol I/O:**
  - 1 SPI / UART
  - 1 I2C
  - 5 GPIO
  - 1 DMA
  - 2 OC/PWMs
  - 1 TMR
  - 2 INTs

- **Logic Analyzer:**
  - 10 GPIO
  - 1 TMR Shared
  - 1 DMA Shared
  - 1 INT

- **Triggering:**
  - 2 GPIO
  - 1 INT

- **USB via UART:**
  - 1 UART
  - 2 DMAs

- **USB: FTDI**
  - (USB for Serial COM)

- **uSD:**
  - 1 SPI

- **WiFi:**
  - 1 SPI / INT
Analog Input

Stage 2 Offset Summing Resistors

PWM Offset Control

Stage 1 Analog Input 1/5 Gain 1M impedance

Stage 2 Feedback Resistors Net Gains 3/40 1/8 1/4 1

1.5V Stage 2 Analog, Offset, Bias Summing Node

Stage 2, Input Summing Resistor

Stage 2 Bias Control

Bias Shift to 1.5V

Stage 2 1.5V Ref

Stage 2 OpAmp

PIC32 ADC 0~3V Centered at 1.5V
Pseudo AC Coupling

- No AC coupling, direct DC coupling.
- Input offset bias via PWM8 allows for pseudo AC coupling.
- Small P2P offset signals can be centered on the MZs ADC input.
Typical Unity Gain Response

-3db ~2.9MHz
3/40 Gain

-3dB ~3.5MHz
Analog In

\[ V = A \cdot D_{\text{adc}} + B \cdot D_{\text{pwm}} - C \]

\[ \mu V_{\text{in}} = (1000000)(3/4096)(R_{31}/R_{30})(R_{32}/R_{1Sx})D_{\text{adc}} \]
\[ + (1000000)(3.3/330)(R_{25}/(R_{22}+R_{23}+R_{25}))(R_{31}/R_{30})(R_{32}/R_{2Sx})D_{\text{pwm}} \]
\[ - (1000000)(R_{31}/R_{30})(R_{32}/R_{2Sx})V_{\text{Ref1.5}} \]

\[ \mu V_{\text{in}} = (13,183,593.75/R_{1Sx})D_{\text{adc}} \]
\[ + (154,338,032.2627525069030664147653/R_{2Sx})D_{\text{pwm}} \]
\[ - (27,000,000,000/R_{2Sx}) \]

Gain 1; \quad A = 732.4, \quad B = 151,311.8, \quad C = 26,470,588.2

Gain 1/4: \quad A = 2,910.3, \quad B = 112,655.5, \quad C = 19,708,029.2

Gain 1/8: \quad A = 5,833.4, \quad B = 64,307.5, \quad C = 11,250,000

Gain 3/40: \quad A = 9,912.5, \quad B = 15,433.8, \quad C = 2,700,000
Calibration

Connect a DC_{out} to the analog input (V_{in})

Hold D_{pwm} constant, vary V_{in} via the DC_{out}
\[ \mu V_{in1} = A \cdot D_{adc1} + B \cdot D_{pwm1} - C \]
\[ -\mu V_{in2} = -A \cdot D_{adc2} - B \cdot D_{pwm1} + C \]

\[ \mu V_{in1} - \mu V_{in2} = A \cdot (D_{adc1} - D_{adc2}) \]

A = \frac{\mu V_{in1} - \mu V_{in2}}{D_{adc1} - D_{adc2}}

Hold V_{in} constant, vary D_{pwm}:
\[ \mu V_{in1} = A \cdot D_{adc1} + B \cdot D_{pwm1} - C \]
\[ -\mu V_{in1} = -A \cdot D_{adc2} - B \cdot D_{pwm2} + C \]

\[ 0 = A \cdot (D_{adc1} - D_{adc2}) + B \cdot (D_{pwm1} - D_{pwm2}) \]

B = A \cdot \frac{D_{adc2} - D_{adc1}}{D_{pwm1} - D_{pwm2}}

C = A \cdot D_{adc1} + B \cdot D_{pwm1} - \mu V_{in1}
Question: How Good is the Uncalibrated Hardware?

a) Within 1%
b) Within 3%
c) Within 5%
d) Within 10%
e) Within 20%
f) Within 50%
g) Worse than 50%
# Actual Instrument Results

### OSC1 calibration constants

\[ u_{\text{In}} = (A \cdot D_{\text{adc}}) + (B \cdot \text{pwm}) - (C) \]

<table>
<thead>
<tr>
<th>Parameters for ( G_x = 1 )</th>
<th>Actual</th>
<th>Ideal</th>
<th>%Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>731.</td>
<td>733.</td>
<td>0.27%</td>
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<tr>
<td>B</td>
<td>150564.</td>
<td>151312.</td>
<td>0.49%</td>
</tr>
<tr>
<td>C</td>
<td>26479038.</td>
<td>26470588.</td>
<td>-0.03%</td>
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</table>

<table>
<thead>
<tr>
<th>Parameters for ( G_x = 2 )</th>
<th>Actual</th>
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<th>%Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2916.</td>
<td>2911.</td>
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<tr>
<td>B</td>
<td>111801.</td>
<td>112656.</td>
<td>0.76%</td>
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<td>C</td>
<td>19661659.</td>
<td>19708029.</td>
<td>-0.24%</td>
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</table>

<table>
<thead>
<tr>
<th>Parameters for ( G_x = 3 )</th>
<th>Actual</th>
<th>Ideal</th>
<th>%Error</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>5807.</td>
<td>5835.</td>
<td>0.48%</td>
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<tr>
<td>B</td>
<td>63670.</td>
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<td>0.99%</td>
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<tr>
<td>C</td>
<td>11193353.</td>
<td>11250000.</td>
<td>0.50%</td>
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<table>
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<tr>
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<th>%Error</th>
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<tbody>
<tr>
<td>A</td>
<td>9855.</td>
<td>9915.</td>
<td>0.61%</td>
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<tr>
<td>B</td>
<td>15392.</td>
<td>15434.</td>
<td>0.27%</td>
</tr>
<tr>
<td>C</td>
<td>2700878.</td>
<td>2700000.</td>
<td>-0.29%</td>
</tr>
</tbody>
</table>

### OSC2 calibration constants

\[ u_{\text{In}} = (A \cdot D_{\text{adc}}) + (B \cdot \text{pwm}) - (C) \]

<table>
<thead>
<tr>
<th>Parameters for ( G_x = 1 )</th>
<th>Actual</th>
<th>Ideal</th>
<th>%Error</th>
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<th>%Error</th>
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<th>%Error</th>
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<td>B</td>
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<td>C</td>
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<td>11250000.</td>
<td>0.00%</td>
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<tr>
<td>C</td>
<td>2711626.</td>
<td>2700000.</td>
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Open Scope Agenda

- Open Scope Waveforms Live Demonstration
- Architecture
- Resource Allocation
- DC Outputs
- Precision Analysis
- Analog Inputs
- **DMA Parallel Processing**
- ADC Interleaving
- Logic Analyzer (LA)
- Scope Triggering
- Analog Waveform Generator (AWG)
- Priority and Stalling Consequences
- USB/Serial, UART Interface
- Open Scope Text Based Protocol
- Building the Sources
DMA Parallel Processing

15 Minute Break
DMA Usage

PIC32MZ2048EFG124

- MUX Select:
  - 4 GPIO
- Channel 1 / 2:
  - 2 OC/PWMs
  - 3 TMRs
  - 4 DMAs
  - 4 Ded. ADCs
- Protocol I/O:
  - 1 SPI / UART
  - 1 I2C
  - 5 GPIO
  - 1 DMA
  - 2 OC/PWMs
  - 1 TMR
  - 2 INTs
- Logic Analyzer:
  - 10 GPIO
  - 1 TMR Shared
  - 1 DMA Shared
  - 1 INT
- DC Generators:
  - 5 OC/PWMs
  - 2 TMRs
- Triggering:
  - 2 GPIO
  - 1 INT
- USB via UART:
  - 1 UART
  - 2 DMAs
- WiFi:
  - 1 SPI / INT
- FTDI (USB for Serial COM)
- uSD
- WiFi
- MRF24

Resource Usage Summary Table

<table>
<thead>
<tr>
<th>Resource</th>
<th>PIC32MZ2048EFG124</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM / OC</td>
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<td>SPI</td>
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<td>Digital Compare</td>
<td>2 of 6</td>
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<tr>
<td>Digital Filters</td>
<td>1 of 6</td>
</tr>
</tbody>
</table>

Analog Inputs

- +/-20V 2 Channels 1 MHz BW

DC Outputs

- 5 DC Outputs from PWMs
- 2 Channels -4V to +4V
- +/-3V 1 Channel 10 MS/s

AWG Output

- MCP6H91
- R2R Ladder
- 10 bit Port H

PWM / OC

- LMV116 / Op Amp
- TS3A5017 / MUX
- MCP6H82 / LMV324IDT
- LM4040AIM3
- 5 PWM
- 2 Ch

2 Offsets

EXT Trigger

Button

PGM Button

Reset Button

High Precision 3V Ref

10 LA Inputs

Port E 10 MS/s

Port F

8 Feedback ADC

- 2 DC
- 1 AWG
- 5 Supply/Ref

10 LA Inputs

1 Channel 10 MS/s

 dissemination 

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DMA Usage

- DMA allows for background processing freeing the CPU to do other things.
- DMA works in parallel with the CPU.
- DMA can be triggered on any interrupt (event) and doesn’t require interrupt routines (ISRs).
- DMA can access peripherals and memory at speeds well surpassing the CPU or ISRs.
PIC32 Cache Considerations

- Default memory allocation is in memory section KSEG0 whose data can be stored in the cache.
- The CPU cache is not updated when data is transferred via DMA.
- DMA Buffers must be allocated in the KSEG1 region whose data will NOT be stored in the cache.
- Cache coherency must be considered.
DMA Observations

- DMA Transfers To/From Non-Cached Memory
  - Declare buffers as `__attribute__((coherent))` to ensure the compiler creates KSEG1 (non-cached) references to the Memory.
  - If reading from cached memory (normal addressing) you may not get the correct values.
  - A trick is to `memcpy()` to/from KSEG0/KSEG1 to ensure both cached and non-cached memory is the same; however this will slow down your code.
  - MPLAB® X IDE only sees cached memory, irrespective of the addressing mode you select.
DMA Observations (continued)

- **Max Cell Triggering <15MT/s**
  - Reduces to about 10MT/s when using multiple DMA channels
  - Triggers are missed if triggered too fast

- **Max DMA Block Size <64K**
  - Destination/Source size of 64K (set to a value of 0) degrades DMA performance substantially and interferes with other channels.

- **All Cell Transfers are Serialized**
  - The highest priority DMA stalls all other channels during the cell transfer time.
  - Irrespective of the buses in use.
ADC Interleaving
ADC Interleaving

 PIC32MZ2048EFG124

- MUX Select: 4 GPIO
- Channel 1 / 2: 2 OC/PWMs, 3 TMRs, 4 DMAs, 4 Ded. ADCs
- Protocol I/O: 1 SPI / UART, 1 I2C, 5 GPIO, 1 DMA, 2 OC/PWMs, 1 TMR, 2 INTs
- Logic Analyzer: 10 GPIO, 1 TMR Shared, 1 DMA Shared, 1 INT
- DC Generators: 5 OC/PWMs, 2 TMRs
- Triggering: 2 GPIO, 1 INT
- USB via UART: 1 UART, 2 DMAs
- uSD: 1 SPI
- WiFi: 1 SPI / INT

Port F
10 LA Inputs
Port E
10 MS/s
EXT
Trigger

PIC32
Resource Usage
Summary Table

<table>
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<tr>
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</tbody>
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Analog Inputs

- +/-20V
- 2 Channels
- 1 MHz BW

DC Outputs

- +/-20V
- 2 Channels
- -4V to +4V
- -/+3V

5 DC Outputs from PWMs

- 5 PWM

5 DC Outputs from PWMs

- 5 PWM

ADC Output

- 10 LA

AWG

- 10 bit
- Port H

AWG: 1 TMR Shared, 1 DMA Shared, Port H

PWM / OC

- 9 of 9

Timers

- 7 of 9

INTs

- 5 of 5

SPI

- 3 of 6

UART

- 2 of 6

I2C

- 1 of 5

DMAs

- 9 of 8

Dedicated ADCs

- 4 of 5

Shared ADCs

- 8 of 43

Digital Compare

- 2 of 6

Digital Filters

- 1 of 6

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Interleaving ADCs

Contrary to Documentation the ADC triggers on the rising edge of OC, or OCxR Match.

SYSCLK

PBCLK3

200MHz

\[ \div 2 \]

100MHz

TMR3

OC5R

OC5R

OC5

PR3

PR3

Triggers 2 PBs after PR Match

OC5R

Triggers 3 PBs after OCxR Match

Contrary to Documentation the ADC triggers on the rising edge of OC, or OCxR Match.
ADC Observations

- **Toss the First Conversion**
  - For an unknown reason, whenever the ADC sit unused for a few milliseconds, the first conversion will be off. The solution is to run the ADC and toss one or more conversions.

- **ADCs OC event is on OCxR Match**
  - The OC documentation says the interrupt is on the failing edge of the OC, or on OCxRS Match; but the ADC is connected directly to the rising edge of the OC.
Correct Interleaving
Improper Interleaving timing
Interleaving out of Sync
Logic Analyzer
Logic Analyzer

Timer 7 and DMA 7 are shared with the AWG
LA Limitations

- **Maximum Sample rate is 10MS/s**
  - The max speed we can trigger a DMA off of a timer is 10MS/s before saturating the DMA trigger.
  - IO Bus is capable of running at 50MS/s. However, only 1 DMA cell transfer can run at a time and running the LA at 50MS/s would stall all other DMAs, including the UART DMA which would stop all communication.

- **Must run at highest DMA priority**
  - To ensure that transfers are not stalled by other DMAs or skew sample timing.
Scope Triggering
Scope Triggering

**Resource Usage Summary Table**

<table>
<thead>
<tr>
<th>Feature</th>
<th>PIC32MZ2048EFG124</th>
<th>PIC32MZ2048EFG124</th>
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</table>

**DC Outputs**

- 5 DC Outputs from PWMs
- 2 Channels
- -4V to +4V
- 2 Offsets

**Analog Inputs**

- +/-20V
- 2 Channels
- 1 MHz BW

**AWG Output**

- MCP6H91
- R2R Ladder
- 10 bit
- Port H

**AWG**

- 2 Ch
- High Precision 3V Ref

**DC Generators**

- 5 DC Outputs from PWMs
- 2 TMRs

**8 Feedback ADC**

- 2 DC
- 1 AWG
- 5 Supply/Ref

**PWM**

- 2 Channels
- DC Outputs
- 2 Offsets

**MCP6H82 / LMV324IDT**

- 5 PWM

**LMV116 / Op Amp TS3A5017 / MUX**

- 5 DC Outputs from PWMs
- 2 Offsets

**EXF Trigger**

- EXT Trigger
- Button

**Logic Analyzer**

- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

**Triggering**

- 2 GPIO
- 1 INT

**USB via UART**

- 1 UART
- 2 DMAs

**uSD**

- 1 SPI

**WiFi**

- 1 SPI / INT

**PIC32MZ2048EFG124**

- MUX Select:
  - 4 GPIO

- Protocol I/O:
  - 1 SPI / UART
  - 1 I2C
  - 5 GPIO
  - 1 DMA
  - 2 OC/PWMs
  - 1 TMR
  - 2 INTs

- Channel 1 / 2:
  - 2 OC/PWMs
  - 3 TMRs
  - 4 DMAs
  - 4 Dedicated ADCs
Trigger Components

- **Trigger**: Where the trigger conditions are met. This is also the time reference to all acquired data.
- **Point of Interest (POI)**: The users focal point within the data. Usually the center of the scope trace. This is where the user wants to see the signal.
- **Trigger Delay**: The Positive or Negative time between POI and the trigger.
- **Requested Buffer**: The data requested for display. The POI is “usually” scrolled to the center of this buffer.
- **Time synchronization** is always referenced to the trigger, the display buffer is referenced/scrolled to the POI.
• DMA destination size is 65532 bytes, or 32766 samples (32638+64+64) of 16bit ADC data.
• DMA has a maximum destination size of 65536 bytes, but when a full 65536 is specified the DMA “freaks-out” and causes massive DMA stalls. We reduce by 4 bytes to “back-off” the maximum.
• 64 samples (128 bytes) are used as additional pre-trigger samples to warm-up the ADC and to ensure good data is in the buffer.
• 64 samples (128 bytes) are used as overrun slop to allow for additional DMA transfers between when the termination timer fires and the interrupt routines stops DMA transfers.
• The WFL request buffer overlays the start of the Acquisition Buffer.
Because it is not known when the Trigger will occur, acquisition must run continuously before the trigger.

Acquisition must run without the trigger enabled to ensure the minimum pre-trigger data is collected.

Acquisition must continue to run until all post-trigger data is collected.
Trigger/POI Implications

- Cannot have POI any further back than your acquisition buffer size.

- If POI is delayed more than your acquisition buffer size, the Trigger will not be retained.
Timing, Acquisition Termination

- If the positive delay is larger than the acquisition buffer, timing between the trigger to the POI must be maintained. Modulo math is used to maintain timing of the trigger and POI. All timing is based off of the trigger.

- End of Acquisition is usually after the POI to fill out the display. The termination timer determines when acquisition stops.

- Trigger and POI indexes in the requested buffer are pre calculated. The actual modulo trigger (and data) is scrolled to the pre calculated trigger index in the buffer at the end of acquisition.
Oscilloscope Threshold Triggers

- Uses ADC hardware Digital Comparator and Interrupts

- **Rising Edge**, (falling Edge, Thresholds switched)
  - Interrupt 1, below lower threshold.
  - Interrupt 2, above upper threshold.
    - This is the trigger, DMA pointers saved.
    - Delay Timer9 is started.
    - Search back in buffer for actual trigger.
  - Interrupt 3, Timer9 expires.
    - Acquisition has ended.
    - All DMA transfers are stopped.
Logic Analyzer Change Notice Triggers

- Uses I/O Port Change Notice and Interrupts
- Rising/Falling/Either Edge
  - Interrupt 1, does not exist.
  - Interrupt 2, Change Notice Event.
    - This is the trigger, DMA pointers saved.
    - Delay Timer9 is started.
    - Search back in buffer for actual trigger.
  - Interrupt 3, Timer9 expires.
    - Acquisition has ended.
    - All DMA transfers are stopped.
Supported Triggers

● Oscilloscope
  ● Rising or Falling Edge Triggers.
  ● Rise / Fall Time with lower and upper threshold.
  ● By default WFL sets the lower threshold 30mV below the upper threshold.

● Logic Analyzer
  ● Rising, Falling, or Either Edge Triggers.
  ● 10 LA signal channels.
  ● Any combination of LA pins can be Triggers.
  ● Pattern matching is not supported.
Multi-Instrument Timing

- Digital Compare Interrupt
- ADC Completion
- Start DMA Transfer
- ADC Trigger ISR

OSC Data Saved in RAM

LA Data saved in acquisition buffer 320ns before the OSC data does!

LA ISR starts execution 320ns + T-SAMP before the OSC ISR
Multi-Instrument Compensation

- All OSC data in the acquisition buffer is 320ns later than data in the LA buffer.
  - The conversion time of the ADC, 1/3,125,000
  - To sync the data, we must move the OSC back 320ns, or the LA forward 320ns when comparing the 2 buffers.

- The ISR synchronizes the DMA pointers.
  - All DMA pointers for all instrument acquisition buffers are snapshot. Then time adjusted for the OSC/LA.
  - The ISR must look back in the buffer to find the actual trigger. All other instrument pointers must be adjusted.
  - At very low sample rates (T-SAMP >> T-Prolog) it is possible that the LA ISR can execute before the DMA transfers the data to RAM. The PORT register must be considered when finding the actual trigger.
Analog Waveform Generator (AWG)
Analog Waveform Generator (AWG)

- **PIC32MZ2048EFG124**
  - Protocol I/O:  
    - 1 SPI / UART  
    - 1 I2C  
    - 5 GPIO  
    - 1 DMA  
    - 2 OC/PWMs  
    - 1 TMR  
    - 2 INTs
  - Logic Analyzer:  
    - 10 GPIO  
    - 1 TMR Shared  
    - 1 DMA Shared  
    - 1 INT
  - USB via UART:  
    - 1 UART  
    - 2 DMAs
  - WiFi:  
    - 1 SPI / INT

- **Resource Usage Summary Table**
  - PWM / OC: 9 of 9  
  - Timers: 7 of 9  
  - INTs: 5 of 5  
  - SPI: 3 of 6  
  - UART: 2 of 6  
  - I2C: 1 of 5  
  - DMAs: 9 of 8  
  - Dedicated ADCs: 4 of 8  
  - Shared ADCs: 8 of 43  
  - Digital Compare: 2 of 6  
  - Digital Filters: 1 of 6

- **ANALOG INPUTS**
  - +/-20V  
    - 2 Channels  
    - 1 MHz BW

- **DC Outputs**
  - +/-3V
  - 2 Channels
  - -4V to +4V

- **AWG Outputs**
  - 10 MS/s

- **AWG:***
  - 1 TMR Shared  
    - 1 DMA Shared  
    - Port H

- **DC Generators:**
  - 5 OC/PWMs  
    - 2 TMRs

- **8 Feedback ADC**
  - 2 DC  
    - 1 AWG  
    - 5 Supply/Ref

- **PWM / OC**
  - 9 of 9

- **GPIO**
  - 10 GPIO

- **MRF24 WiFi**

- **EXT Trigger**

- **Logic Analyzer**
  - 10 GPIO  
    - 1 TMR Shared  
    - 1 DMA Shared  
    - 1 INT

- **Triggering**
  - 2 GPIO  
    - 1 INT

- **USB**
  - 1 SPI

- **Digital Compare**
  - 2 of 6

- **Digital Filters**
  - 1 of 6
Function Generator

- **R2R 750 Ω Impedance**
- **R Input 4450 Ω Impedance**
- **Summing Node**
- **Reconstruction Filter**
- **PWM Offset Control 2.5V Swing**
- **DAC Output**
- **PWM Gain** 
  \((-4125/3439)\sim(-1.2)\)
  \(1.2\times2.5 = 3\) or +/- 1.5V
- **R2R Gain** 
  \((-4125/4450)\sim(-0.92)\)
  \(3.3V\times0.92 \sim 3.06\) or +/- 1.503V

- **Output Bias** 
  3.3/2V R2R & 1.75V PWM Yields 0V Output

- **PIC32 Output** 
  0 or 3.3V
\[ \text{AWG: } V = -A \cdot D_{\text{dac}} - B \cdot D_{\text{pwm}} + C \]

\[
V_{\text{out}} = -R_{64} / (R_{60} + R_{62} + R_{63}) \cdot V_{\text{cc}} \cdot D_{\text{dac}} / 1024 - R_{64} / (R_{57} + R_{58} + R_{59}) \cdot V_{\text{cc}} \cdot D_{\text{pwm}} / 330 \\
+ R_{64} / (R_{60} + R_{62} + R_{63}) \cdot V_{\text{Ref1.5}} + R_{64} / (R_{57} + R_{58} + R_{59}) \cdot V_{\text{Ref1.5}} \\
+ (V_{\text{Ref1.5}} - V_{\text{Ref3.0}}) \cdot R_{64} / (R_{66} + R_{67}) + V_{\text{Ref1.5}}
\]

\[
V_{\text{out}} = -4125 / 4450 / 1024 \cdot V_{\text{cc}} \cdot D_{\text{dac}} - 4125 / 3439 / 330 \cdot V_{\text{cc}} \cdot D_{\text{pwm}} + 2.130161 + 1.5
\]

\[ A \approx 0.002987; \ B \approx 0.011995; \ C \approx 3.630161 \]

\[ \mu V_{\text{out}} \approx -2987 \cdot D_{\text{dac}} - 11995 \cdot D_{\text{pwm}} + 3630161 \]

-2987 \cdot D_{\text{dac}} implemented via best fit table lookup

\[ \mu V_{\text{PWM Offset}} = 0; \text{ When } D_{\text{pwm}} = 175; \]

\[ \mu V_{\text{PWM Offset}} = -11995 \cdot D_{\text{pwm}} + 2099125 \]
AWG Calibration

- Only the PWM Offset Coefficients are calibrated.
- Coefficient for the R2R ladder is NOT calibrated.
- Each voltage code is applied and then read via the feedback network.
- The read codes are sorted.
- A best fit sorted lookup table is used to determine which code to use for a specific voltage.
Waveform Generator

Index of Closest Voltage used to Lookup R2R Code

Sort Sorted R2R Code Lookup Table
1024 Entries, Cached KSEG 0

R2R Code 0
R2R Code 1
R2R Code 2
......
......
R2R Code 1020
R2R Code 1021
R2R Code 1022
R2R Code 1023

PBCLK3
200MHz ÷2
100MHz

SYSCLK

TMR7

DMA7

Port H

Timer 7 and DMA 7 are shared with the LA

Pre-Generated Waveform R2R Code Table
Non-cached KSEG 1

CHAEN

Best Fit Sorted Voltage Feedback Lookup Table
1024 Entries Cached KSEG 0

mVolt 0
mVolt 1
mVolt 2
mVolt 3
mVolt 4
mVolt 5
......
......
mVolt N

-1500mV
-1498mV
-1495mV
......
0mV
......
1493mV
1497mV
1500mV

mVolt 0
mVolt 1
mVolt 2
mVolt 3
mVolt 4
mVolt 5
......
......
"mVolt N"

-1500mV
-1498mV
-1495mV
......
0mV
......
1493mV
1497mV
1500mV

mVolt 0
mVolt 1
mVolt 2
mVolt 3
mVolt 4
mVolt 5
......
......
"mVolt N"
R2R Ladder is not Precise

- Only 1% resistors are used.
- It is possible to have missing codes.
  - For example if when switching from 0x1FF to 0x200 if that step is greater than 3mv, there is no way to pick up the missing LSB.
- There is a propagation delay through the ladder that causes switching spikes.
  - Most noticeable when switching from/to 0x1FF <-> 0x200
Accommodate Missing Codes
Transmission Delay in the R2R Ladder
Simulated Transmission Delay

![Graph showing simulated transmission delay]
Actual Transmission Delay
Or you can buy a DAC

50kHz Sine, 200mVpk-pk, 100mV/div, (1000 unit pricing)
blue – DAC7822 ($4.28)
yellow – AD5405 ($6.62)

OpenScope R2R Ladder/MCP6H91 ($1.06)
Open Scope Agenda

- Open Scope Waveforms Live Demonstration
- Architecture
- Resource Allocation
- DC Outputs
- Precision Analysis
- Analog Inputs
- DMA Parallel Processing
- ADC Interleaving
- Logic Analyzer (LA)
- Scope Triggering
- Analog Waveform Generator (AWG)

Priority and Stalling Consequences

- USB/Serial, UART Interface
- Open Scope Text Based Protocol
- Building the Sources
Priority and Stalling Consequences

15 Minute Break
Priority and Stalling

PIC32MZ2048EFG124

MUX Select:
- 4 GPIO

Channel 1 / 2:
- 2 OC/PWMs
- 3 TMRs
- 4 DMAs
- 4 Ded. ADCs

Protocol I/O:
- 1 SPI / UART
- 1 I2C
- 5 GPIO
- 1 DMA
- 2 OC/PWMs
- 1 TMR
- 2 INTs

Logic Analyzer:
- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

Triggering:
- 2 GPIO
- 1 INT

USB via UART:
- 1 UART
- 2 DMAs

uSD:
- 1 SPI

WiFi:
- 1 SPI / INT

Resource Usage Summary Table

<table>
<thead>
<tr>
<th>Resource Type</th>
<th>PIC32MZ2048EFG124</th>
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MVP116 / Op Amp
TS3A5017 / MUX

Analog Inputs

+/-20V
2 Channels
1 MHz BW

DC Outputs

2 Channels
-4V to +4V

5 DC Outputs from PWMs

MCP6H82 / LMV324IDT

2 Offsets

Button

EXT Trigger

Port F

Port E
10 Inputs
10 MS/s

DC Generators:
- 5 OC/PWMs
- 2 TMRs

High Precision
3V Ref

8 Feedback ADC
- 2 DC
- 1 AWG
- 5 Supply/Ref

5 PWM

2 Ch

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MASTERs 2017

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DMA Stalling

- Experimentally, maximum cell transfer tops out at <15MTrig/s, and more like 10MTrig/s if multiple DMAs are in use. Cell transfer triggers are missed (not queued) if the trigger rate is exceeded.
- Only the highest priority DMA cell transfer will run at a time regardless of busses in use; all other DMAs will stall.
- Various system busses have different DMA speeds. IO Bus at 50MTran/s, RAM to RAM at 100MTran/s.
- A transfer is the cell size or 32bits, whichever is smaller.
- The current transfer will complete before a higher priority DMA will be allowed to run.
DMA Priority

- **Top priority to the AWG & LA (10MT/s)**
  - In order to read (LA) or write (AWG) samples at extremely regular rates, the AWG/LA must not be stalled. Stalls cause distortions in the waveform.
  - Both the AWG and LA use the IO bus and have top priority, so they can not run at the same time, or one would stall the other.

- **Next priority to Analog-In (3.125MT/s)**
  - We have up to the conversion time, 320ns, for the DMA to transfer the ADC result to RAM.

- **UART has lowest priority (139kT/s)**
  - The UART has an 8 byte FIFO and runs at 139kTran/s. There is lots of time to keep up.
Interrupt Priorities

- Minimal interrupts in the system
  - Trigger Interrupts
    - Priority 7, Trace competition interrupt on TMR9.
    - Priority 6, Trigger detection interrupt
      - OSC, Digital Compare threshold INT.
      - LA, Change Notice INT.
    - Priority 5, OSC pre-threshold INT.
  - WiFi Interrupt
    - Priority 3, MRF24 WiFi Data Ready INT.
USB/Seral, UART Interface
USB / Serial Interface

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<tr>
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**MCP6H82 / LMV324IDT**

- 5 DC Outputs from PWMs
- 2 Channels
- -4V to +4V
- +/-20V
- 2 Channels
- 1 MHz BW
- 2 Offsets

**MCP6H91**

- AWG
- 10 bit
- Port H
- +/-3V
- +/-1.5 Offset
- 1 Channel
- 10 MS/s

**LMV116 / Op Amp**

- TS3A5017 / MUX
- 1
- 4
- 8
- 40

**PIC32MZ2048EFG124**

- MUX Select:
  - 4 GPIO
- Channel 1 / 2:
  - 2 OC/PWMs
  - 3 TMRs
  - 4 DMAs
  - 4 Ded. ADCs
- Protocol I/O:
  - 1 SPI / UART
  - 1 I2C
  - 5 GPIO
  - 1 DMA
  - 2 OC/PWMs
  - 1 TMR
  - 2 INTs
- Logic Analyzer:
  - 10 GPIO
  - 1 TMR Shared
  - 1 DMA Shared
  - 1 INT
- DC Generators:
  - 5 OC/PWMs
  - 2 TMRs
- USB via UART:
  - 1 UART
  - 2 DMAs
- WiFi:
  - 1 SPI / INT
- AWG:
  - 1 TMR Shared
  - 1 DMA Shared
  - Port H
- Button
- PGM Button
- Reset Button
- High Precision 3V Ref
- EXT Trigger
- Port F
- Port E
- 10 LA Inputs
- 10 MS/s
- 10 LA
- Inputs
- 10 LA

**FTDI (USB for Serial COM)**

- uSD
- uSD
- uSD
- FTDI
- MRF24 WiFi
- WiFi
- WiFi
USB/Serial, UART Interface

- **FTDI FT232RQ USB/Serial Converter.**
  - Offloads the USB stack to the FTDI chip.
  - Runs at 1.25MBaud, 139kB/s.
  - Requires USB 2.0 High Speed or better.
  - Provides text communication via Terminal.
    - Menu Mode
    - JSON Mode
  - Negotiates 500mA on the USB bus.
  - Provides the board Serial Number during enumeration in Device Instance Path / Parent
DMA and the UART

Serial.available() = DCH0DPTR – pLastRead;

Input Buffer

Byte 0
Byte 1
Byte 2
Byte 3
Byte ..
Byte N

Output Buffer

Byte 0
Byte 1
Byte 2
Byte 3
Byte ..
Byte N

UART5

U5RXREG
FIFO 0
FIFO 1
FIFO 2
FIFO 3
FIFO 4
FIFO 5
FIFO 6
FIFO 7
U5TXREG

DMA0

URXISEL = 0 (INT when not empty)
_UART5_RX_VECTOR

DMA1

UTXISEL = 0 (INT at least 1 empty)
_UART5_TX_VECTOR

Serial.task()
{
    DCH1SSA = pStart;
    DCH1SSIZ = cbWrite;
    DCH1CONbitsCHAEN = 0;
    DCH1CONbits.CHEN = 1;
    pStart += cbWrite;
    cbWrite = 0;
}

Serial.print(sz)
{
    strcpy(pStart + cbWrite, sz);
    cbWrite += strlen(sz);
}
OpenScope Text Based Protocol
Text Based Protocol

PIC32MZ2048EFG124

- MUX Select:
  - 4 GPIO
- Channel 1 / 2:
  - 2 OC/PWMs
  - 3 TMRs
  - 4 DMAs
  - 4 Ded. ADCs
- Protocol I/O:
  - 1 SPI / UART
  - 1 I2C
  - 5 GPIO
  - 1 DMA
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  - 1 TMR
  - 2 INTs
- Logic Analyzer:
  - 10 GPIO
  - 1 TMR Shared
  - 1 DMA Shared
  - 1 INT
- DC Generators:
  - 5 OC/PWMs
  - 2 TMRs
- Triggering:
  - 2 GPIO
  - 1 INT
- USB via UART:
  - 1 UART
  - 2 DMAs
- uSD:
  - 1 SPI
- WiFi:
  - 1 SPI / INT
- EXT Trigger
- Port F
- Port E
- 10 LA Inputs
- 10 MS/s

Analog Inputs
- +/−20V
- 2 Channels
- 1 MHz BW

DC Outputs
- +/−20V
- 2 Channels
- 10 MS/s

PWM / OC
- 9 of 9
Timers
- 7 of 9
INTs
- 5 of 5
SPI
- 3 of 6
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MCP6H82 / LMV324IDT
- 5 DC Outputs from PWMs
- 2 Offsets

MCP6H91
- 10 bit
- Port H

LMV116 / Op Amp
- TS3A5017 / MUX
- 1
- 4
- 8
- 40

5 PWM
- 2 Ch

EXT MUX
- 2 Ch

MRF24 WiFi
- uSD
- FTDI (USB for Serial COM)
Text Based Protocol

- **Serial and Web Based JSON Commands**
  - Comprehensive JSON/text command set
  - HTTP/HTML Post interface
    - JSON command set in body of Post
  - Serial/COM interface
    - Identical JSON command set sent as serial text.

- **Serial based Debug Prints**
  - Informative debug prints for manual observation of operation.

- **Serial based Menus**
  - Primarily used for early development; later replaced by the JSON commands.
Example JSON Command

Command:
{"awg": "1": [{"command": "getCurrentState"}]}

Response:
{
    "awg": {
        "1": [{
            "command": "getCurrentState",
            "statusCode": 0,
            "wait": 0,
            "state": "running",
            "waveType": "sine",
            "actualSignalFreq": 1000000,
            "actualVpp": 3000,
            "actualVOffset": 0
        }]
    }
}
Terminal/JSON/Command Demo

```
{
  "awg": {
    "1": [
      {
        "command": "getCurrentState",
        "statusCode": 0,
        "wait": 0,
        "state": "running",
        "waveType": "sine",
        "actualSignalFreq": 1000000,
        "actualVpp": 3000,
        "actualVOffset": 0
      }
    ]
  }
}
```

USB/Serial
OpenScope HTTP Interface
HTTP Interface

**Resource Usage Summary Table**

<table>
<thead>
<tr>
<th>Component</th>
<th>PIC32MZ2048EFG124</th>
<th>PIC32</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PWM / OC</strong></td>
<td>9 of 9</td>
<td>10 LA Inputs</td>
</tr>
<tr>
<td><strong>Timers</strong></td>
<td>7 of 9</td>
<td>Port F</td>
</tr>
<tr>
<td><strong>INTs</strong></td>
<td>5 of 5</td>
<td>Port E</td>
</tr>
<tr>
<td><strong>SPI</strong></td>
<td>3 of 6</td>
<td>10 MS/s</td>
</tr>
<tr>
<td><strong>UART</strong></td>
<td>2 of 6</td>
<td>EXT Trigger</td>
</tr>
<tr>
<td><strong>I2C</strong></td>
<td>1 of 5</td>
<td></td>
</tr>
<tr>
<td><strong>DMAs</strong></td>
<td>9 of 8</td>
<td></td>
</tr>
<tr>
<td><strong>Dedicated ADCs</strong></td>
<td>4 of 5</td>
<td></td>
</tr>
<tr>
<td><strong>Shared ADCs</strong></td>
<td>8 of 43</td>
<td></td>
</tr>
<tr>
<td><strong>AN Inputs</strong></td>
<td>5 DC Outputs</td>
<td></td>
</tr>
<tr>
<td><strong>DC Outputs</strong></td>
<td>2 DC</td>
<td></td>
</tr>
<tr>
<td><strong>AN Outputs</strong></td>
<td>5 PWM</td>
<td></td>
</tr>
<tr>
<td><strong>DC Generators</strong></td>
<td>5 DC Outputs</td>
<td></td>
</tr>
<tr>
<td><strong>8 Feedback ADC</strong></td>
<td>2 DC</td>
<td></td>
</tr>
<tr>
<td><strong>USB via UART</strong></td>
<td>1 UART</td>
<td></td>
</tr>
<tr>
<td><strong>uSD</strong></td>
<td>1 SPI</td>
<td></td>
</tr>
<tr>
<td><strong>WiFi</strong></td>
<td>1 SPI / INT</td>
<td></td>
</tr>
<tr>
<td><strong>Logic Analyzer</strong></td>
<td>10 GPIO</td>
<td></td>
</tr>
<tr>
<td><strong>Triggering</strong></td>
<td>2 GPIO</td>
<td></td>
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</table>

**PWM / DC Outputs**

- LMV116 / Op Amp
- TS3A5017 / MUX
- MCP6H82 / LMV324IDT
- PIC32MZ2048EFG124

**DC Outputs**

- 2 Channels -4V to +4V
- +/-20V 2 Channels 1 MHz BW

**AN Outputs**

- 2 Ch
- 5 PWM
- 2 Offsets
- MUX

**AN Inputs**

- 5 DC Outputs from PWMs
- 2 Ch
- +/3V +/-1.5 Offset 1 Channel 10 MS/s
- 5 PWM
- 2 Ch

**逻辑分析仪**

- 10 GPIO
- 1 TMR
- 1 DMA
- 1 INT

**USB/串行 COM**

- 1 UART
- 2 DMAs

**数字比较器**

- 2 of 6

**数字滤波器**

- 1 of 6

**逻辑位**

- MRF24 WiFi
- FTDI (USB for Serial COM)
- uSD

**EXT Trigger**

- 2 GPIO
- 1 INT

**复位按钮**

- 1 TMR
- 1 DMA
- Port H

**Port F**

- 10 MS/s

**Port E**

- 10 LA Inputs

**逻辑设计**

- PIC32
- 10 LA
- 10 Inputs

**电路设计**

- 5 DC Outputs from PWMs
- 2 Ch
- +/3V +/-1.5 Offset 1 Channel 10 MS/s
- 5 PWM
- 2 Ch

**逻辑端口**

- Port H
- Port E

**逻辑设计**

- PWM / DC Outputs
- AN Inputs
- AN Outputs

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HTTP Server and Network Stack

- The OpenScope implements a simple HTTP Server.
  - Presented in the 2014 18020 EWN MASTERS class.
  - Supports static web content stored on the uSD card.
  - Supports dynamic content implemented in code.
  - Runs on the Digilent delIP™ Network Stack.
  - Provides the web based interface to the OpenScope.
Connectivity, WiFi, Hotspots, and Isolation
WiFi, Hotspots, and Isolation

PIC32MZ2048EFG124

- MUX Select: 4 GPIO
- Protocol I/O: 1 SPI / UART
- Channel 1 / 2: 2 OC/PWMs
- Logic Analyzer: 10 GPIO
- DC Generators: 5 OC/PWMs
- DC Generator: 2 DC
- USB via UART: 1 UART
- 8 Feedback ADC: 2 DC
- USB: 1 SPI
- AWG: 1 TMR Shared
- WiFi: 1 SPI / INT
- AWG: 1 TMR Shared

Resource Usage Summary Table

<table>
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<tr>
<td>Digital Compare</td>
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<td></td>
</tr>
<tr>
<td>Digital Filters</td>
<td>1 of 6</td>
<td></td>
</tr>
</tbody>
</table>

Analog Inputs

- +/-20V 2 Channels 1 MHz BW
- 5 DC Outputs from PWMs

DC Outputs

- 2 Ch
- 2 DC Outputs -4V to +4V
- 5 PWM

AWG Output

- +/-3V
- 1 Channel 10 MS/s
- 10 LA Inputs

5 DC Outputs from PWMs

- 2 Ch
- 2 Offsets
- 5 PWM

MCP6H82 / LMV324IDT

DC Generators:

- 5 OC/PWMs
- 2 TMRs

USB via UART:

- 1 UART
- 2 DMAs

USB:

- 1 SPI

WiFi:

- 1 SPI / INT

EXT Trigger

- 2 GPIO
- 1 INT

LOGIC ANALYZER:

- 10 GPIO
- 1 TMR Shared
- 1 DMA Shared
- 1 INT

TRIGGERING:

- 2 GPIO
- 1 INT

uSD:

- 1 SPI

MRF24 WiFi

Port E

10 LA Inputs

Port F

10 MS/s

FTDI (USB for Serial COM)

uSD

MRF24 WiFi

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Connecting to WFL

- **http://waveformslive.com**
  - Downloads WFL off of the Digilent Servers

- **http://<OpenScope IP>**
  - Directs to the OpenScope for content.
  - Returns a redirect to http://waveformslive.com
    - The redirect page is stored in flash, there is no need for an uSD card to be present.
    - If the redirect fails, WFL will be served up from the OpenScope uSD, if present.

- **http://<OpenScope IP>/index.html**
  - Forces downloading WFL from the OpenScopes uSD card, if present.
WiFi, Hotspot, and Isolation

- The OpenScope can serve-up WFL.
  - If WFL is stored on the OpenScope’s uSD card.
- WFL works on most Phone Browsers.
  - Your phone can be WFL’s UI.
- The OpenScope can connect to your phone’s Hot Spot for local connectivity.
  - World Wide Internet access is not needed.
- Complete electrical isolation when powering the OpenScope off of a USB battery.
  - Use your OpenScope on a deserted island.
Stand-a-lone Operation

USB Battery Pack

WiFi Wireless Phone Hotspot & Browser

uSD with WFL Content Pages

WiFi Connectivity

Test Circuit Powered by OpenScope
Open Source Hardware and Software
The OpenScope is Open Source

- Firmware is fully open source.
  - Source is free and available on request.
  - All firmware is under MIT or BSD2.
  - There is no GPL/LGPL or other infectious licenses in the firmware.
  - Code can be used for commercial applications without the requirement to source 3rd party proprietary code. Attribution is required.

- Complete Schematics are available.
  - Schematics are posted on our product page.
  - Hardware design is under creative commons.
  - Project/Gerber files are not available.
MPLAB® X IDE
Build Environment
MPLAB® X IDE project

- The OpenScope builds as a Native MPLAB® X IDE Project.
  - In MPLAB® X IDE, Open the OpenScope.X project in the OpenScope directory.
  - If you added the OpenScope directory to your Arduino IDE Sketchbook, you can open the X project directly from the OpenScope directory.

- Install MPLAB® XC32 1.43 compiler.
  - Install MPLAB® XC32 1.43 or newer (free) compiler and assign that compiler to the project.
  - Or use the MPLAB® XC32 1.43 compiler that installed with the Digilent Arduino Core.
MPLAB® X IDE Considerations

- When you program from MPLAB® X IDE, all flash is erased.
  - You will lose calibration and WiFi information stored in flash. You will have to recalibrate and re-add WiFi information.
    - If you use a uSD card, you can save your calibration and WiFi data to the uSD card and you will not have to restore these each time you program. However, your WiFi passphrase will be easily accessible/readable on the uSD card.
  - The project programs the OpenScope’s bootloader so you will not lose the bootloader.
Hardware Programmer

When plugging in the hardware programmer, make sure pin 1 of the programmer, lines up with the square pin on the ICSP connector, JP2.
Arduino IDE
Build Environment
Building with the Arduino IDE

- **Install the Arduino IDE 1.6.9**
  - Newer versions of the IDE may not work.
    - When Arduino.cc and Arduino.org remerged their IDEs, the IDE regressed and does not build subdirectories properly.

- **Install the Digilent Arduino Core**
  - In the Arduino IDE Preferences->Additional Board Managers URLs add:
    - https://s3-us-west-2.amazonaws.com/digilent/Software/Digilent_Core/package_digilent_index.json
  - In the Arduino IDE Tools->Board->Boards Manager
    - Install the Digilent Core
Arduino IDE Considerations

- The OpenScope uses nothing from the Digilent core, almost!
  - The OpenScope sketch is stand-a-lone, nothing from the core is brought in, except, crti.S.
    - When building from MPLAB® X IDE, X provides this file. The Digilent Core, and X provided crti.S are functionally equivalent.
  - Unfortunately, the core is still compiled.
  - OpenScope.ino has no code in it.
    - However, Arduino always compiles the sketch’s .ino file; it still must compile for the OpenScope.
    - The .ino file implicitly includes Arduino.h; however, this contributes nothing to the code.
MPLAB® XC32 Considerations

- Both the Digilent Arduino toolchain and MPLAB® X IDE toolchain use the official Microchip MPLAB® XC32 compiler.
  - Unlike the chipKIT core that uses a special chipKIT compiler, the Digilent core uses the same MPLAB® XC32 compiler as MPLAB® X IDE native builds.
  - The MPLAB® XC32 compiler is used with the –mnewlib-libc option to force the usage of the open source newlib runtime libraries.
  - By default the OpenScope is compiled without optimizations, so the “free” MPLAB® XC32 is used.
  - Both X/Arduino builds generate substantially the same code. (build order and placement may vary).
Resource Links
OpenScope Resource Links

- Digilent: www.digilent.com
- Microchip: www.microchip.com
- Arduino: www.Arduino.cc
- OpenScope Firmware: https://reference.digilentinc.com/reference/instrumentation/openscope-mz/previous-versions
OpenScope Resource Links

- Firmware Source: https://github.com/Digilent/openscope-mz
- Waveformslive Browser Page: https://www.waveformslive.com
OpenScope Resource Links

- MPLAB® X IDE (3.60 or newer): http://www.microchip.com/mplab/mplab-x-ide
- XC32 Compiler (1.43 or newer): http://www.microchip.com/mplab/compilers
- Arduino IDEs (1.6.9) https://www.arduino.cc/en/Main/OldSoftwareReleases#previous
- Digilent Arduino Core https://s3-us-west-2.amazonaws.com/digilent/Software/Digilent_Core/package_digilent_index.json
Open Scope Summary

- Open Scope Waveforms Live Demonstration
- Architecture
- Resource Allocation
- DC Outputs
- Precision Analysis
- Analog Inputs
- DMA Parallel Processing
- ADC Interleaving
- Logic Analyzer (LA)
- Scope Triggering
- Analog Waveform Generator (AWG)
- Priority and Stalling Consequences
- USB/Serial, UART Interface
- Open Scope Text Based Protocol
- Building the Sources
Hope you enjoyed our class..
Appendix
Waveformslive Browser Based User Interface
Waveformslive (WFL) Browser Based UI

- **Written using:**
  - TypeScript, strict superset of JavaScript.
  - Uses the Flot Graphics Package.
  - Ionic 2, built on Angular 2 and utilizes Apache Cordova.
  - Cordova supports the creation of native applications to Android, iOS, Windows, and more.
- **Targets PCs, Tablets, and Phones.**
- **Runs on most Browsers**
  - Chrome, Edge, Firefox, Safari
WFL Communications

- HTTP Posts with an HTML body containing OpenScope JSON commands.
- Binary data is transferred using the HTTP Chunked Transfer Encoding.
- Communicates to the Digilent Agent in an identical manner as the OpenScope; with HTTP Post messages.
  - The Digilent Agent supports a config URL where HTTP Posts with Digilent Agent specific JSON commands can be interpreted.
MASTERs Conference

Digilent Agent
Digilent Agent (DA)

- A local HTTP server forwarding OpenScope commands over the USB/Serial/COM interface.
  - Same HTTP protocol as the OpenScope.
  - Written in QT for cross-platform support.
    - Runs on Windows, MAC, and Linux

- Started out as the OpenScope Configuration Utility to configure WiFi and calibration.
  - Configuration commands were designed as OpenScope JSON commands.
  - The DA can forward on any and all WFL commands enabling USB/Serial connectivity to the OpenScope.
Digilent Agent, Not Just for the OpenScope; Looking Forward

- The DA can convert to other interfaces and protocols.
  - The JSON command set is generic to instrumentation, not specific to the OpenScope.
  - The JSON commands can be translated into Analog Discovery commands and connected to the Analog Discovery via its native Adept protocol.
- WFL can be developed as a generic instrumentation Browser Based UI for many instruments.
- LabVIEW can connect to the DA and communication easily to the AD2 and/or OpenScope.
Enabling WiFi/Internet Connectivity with the DA

- The DA runs as an HTTP server on the PC.
  - The PC is connected to the internet.
  - Anything that is connected to the internet can communicate to the DA.
  - Could make a less expensive OpenScope with no WiFi module and still talk WiFi to it through a DA. Also could enable WiFi access to the AD2.

- WFL is a Web Based Application
  - It is connected to the internet and can communicate with any or many DAs on the internet.
  - Could support multiple instruments over a range of PCs. This could be useful for data collection over a widely distributed instrumentation network.
LC Tank Examples
LC Tank Board Test Points

- Comparator -
- Comparator Out
- LC - Tank
- Comparator +
- Peak Detect
- Op-Amp Out
- Op-Amp -
- GND
- LA - Prox
- Vdd – 4V
- LA - PGD
- LA - PGC
- LA - UART
- MCLR
- Vdd
- GND
LC Tank Schematic and Setup

Demo Procedure:

- Type [www.waveformslive.com](http://www.waveformslive.com) and connect to OpenScope via Digilent Agent to start GUI:

![OpenScope GUI](image)

- Review instruments (time base, trigger, OSC1/2, Wavegen, Digital Logic Analyzer, DC Power)

![Instrument GUIs](image)
Waveform Generator Demo

- Connect AWG to OSC1, set AWG to 100 Khz, 3V P-P, sine Wave

- Increase frequency to 1 Mhz

- Observe ~6 sample points per cycle (1 Mhz input, 6.25 Ms/S)

- Press “Single” and observe captured waveforms on OSC1

- DC Power Supply
  - Ch 1: 3.982 V
  - Ch 2: 26.00 mV
Oscilloscope and FFT Demo

- Connect Power, Ground and OSC1 to LC, OSC2 to Comparator output
- Disable waveform generator
- Set OSC1 to 200 mV
- Set OSC2 to 1V
- Set time base to 2 us/Division

Observe FFT:

- Compare to board measured frequency in terminal program
  - Peak = 891 Diff = 6 0%, LC = 1569 Freq = 401470 Hz Diff = 569 0%
  - Add metal and show frequency change.
Logic Analyzer Demo

- Connect OSC2 to op-amp output:
- Connect logic analyzer to UART TX pin and PROX pins
- Turn on LA 1 and LA2 channels
- Observe serial mixed signal UART LC tank / op-amp data in one place.
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