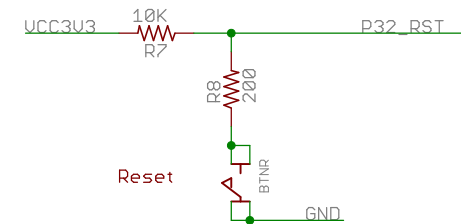
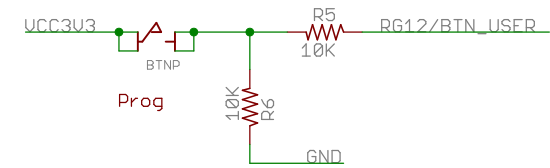
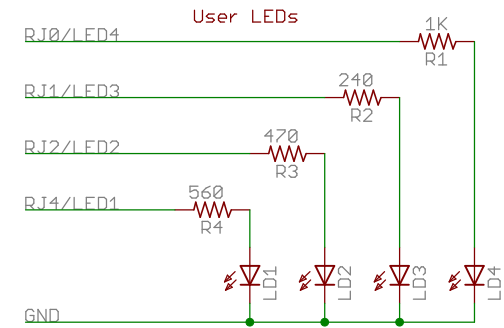
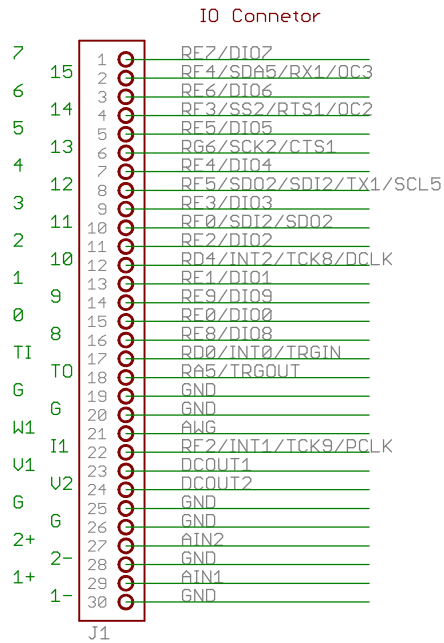


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3	USB and Programming
4	Analog Channel 1
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10	WiFi and uSD Card
11	Feedback Network
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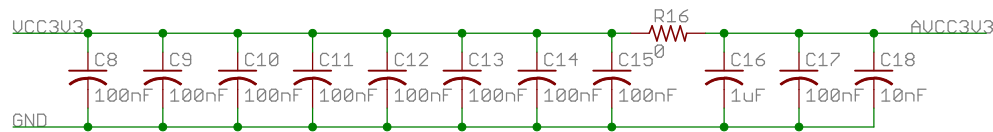
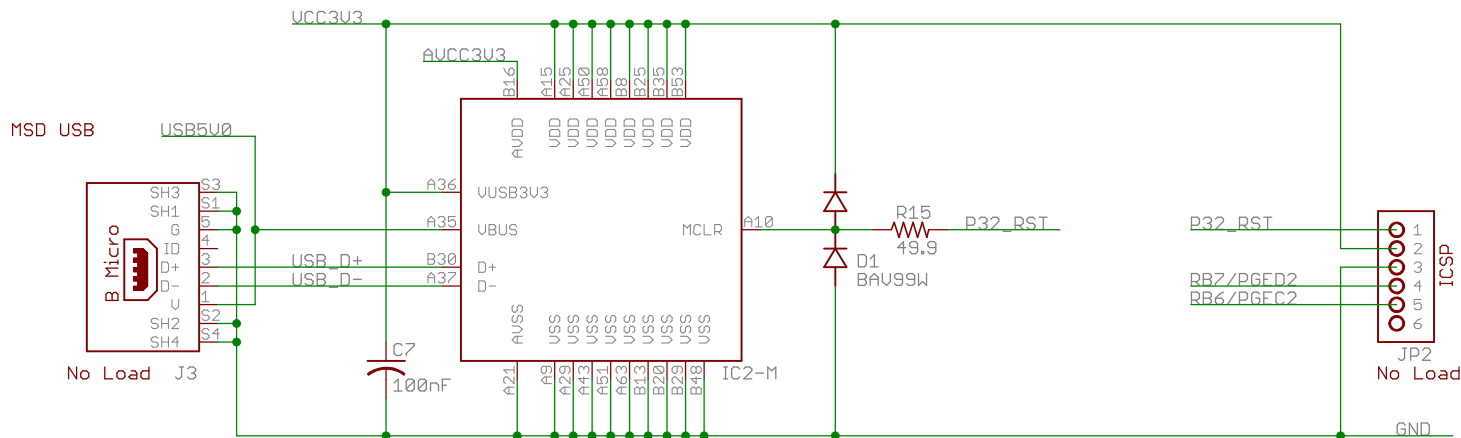
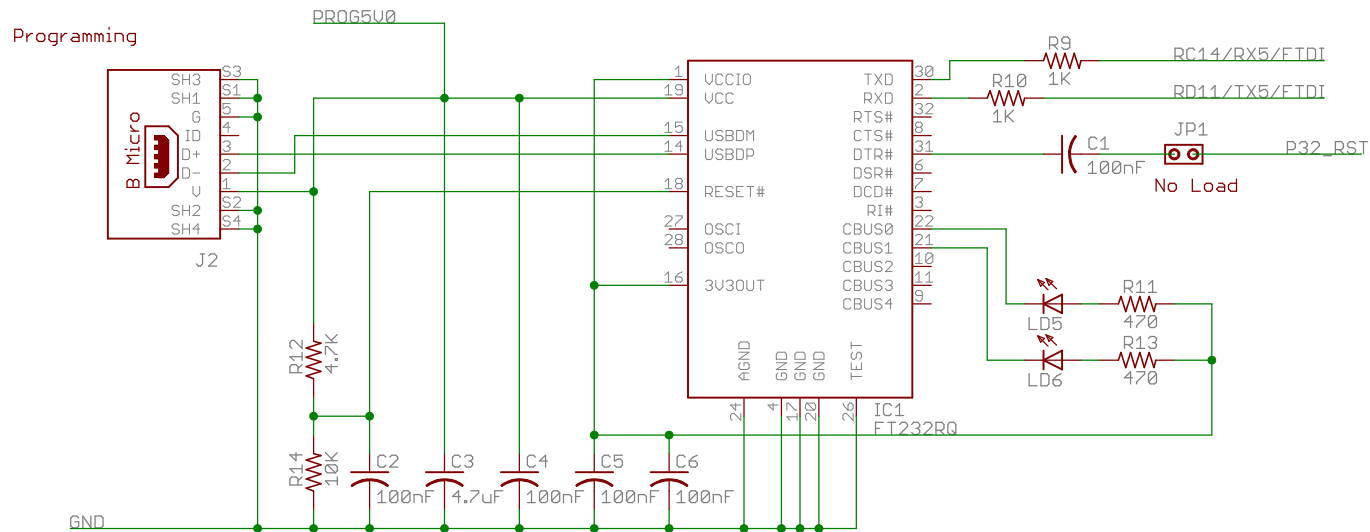
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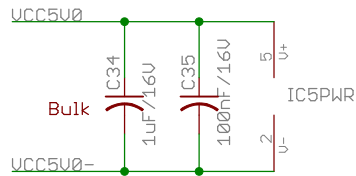
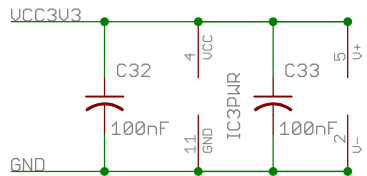
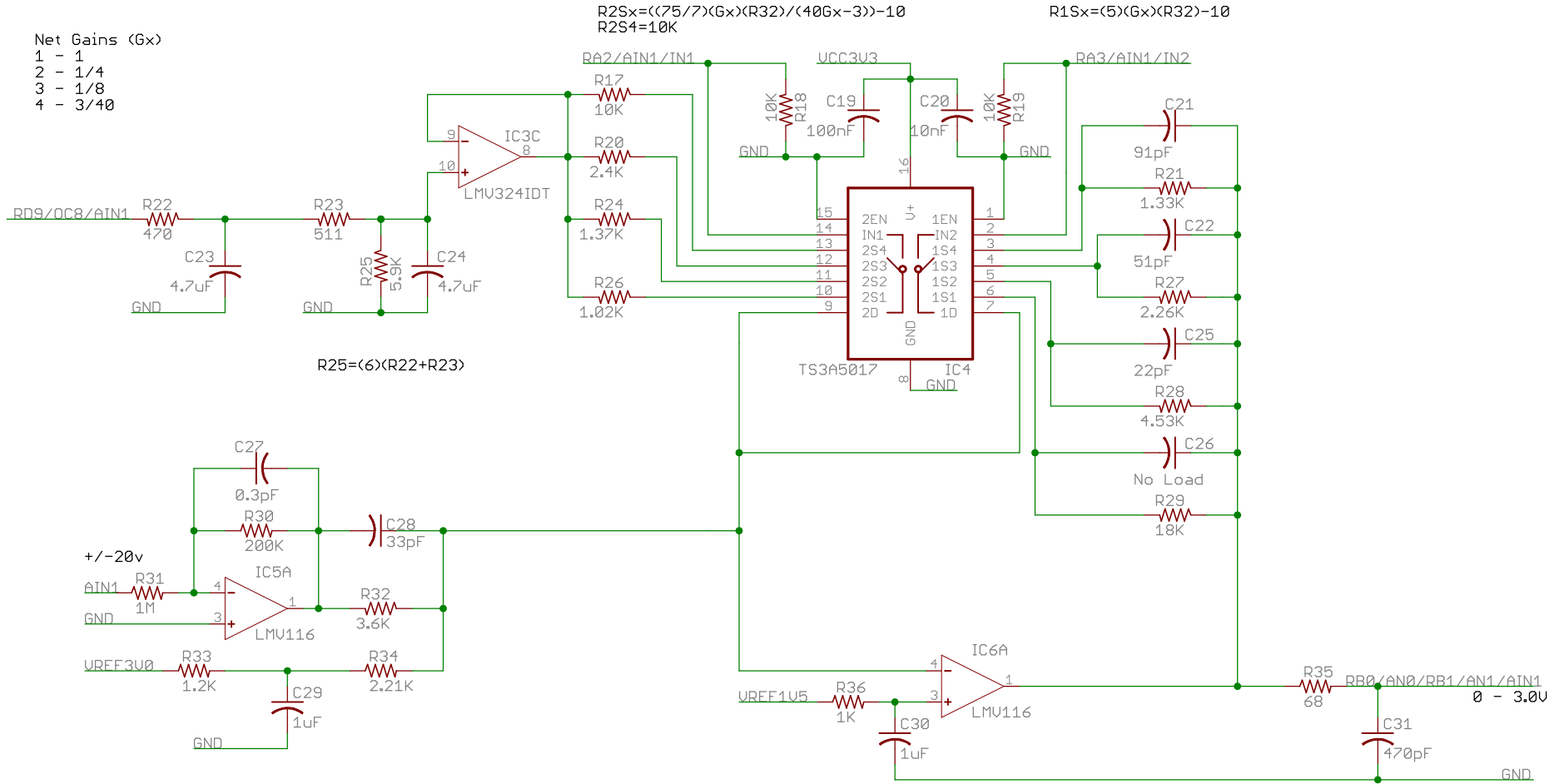
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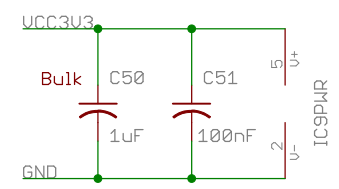
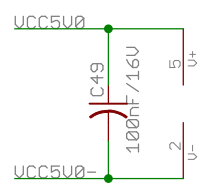
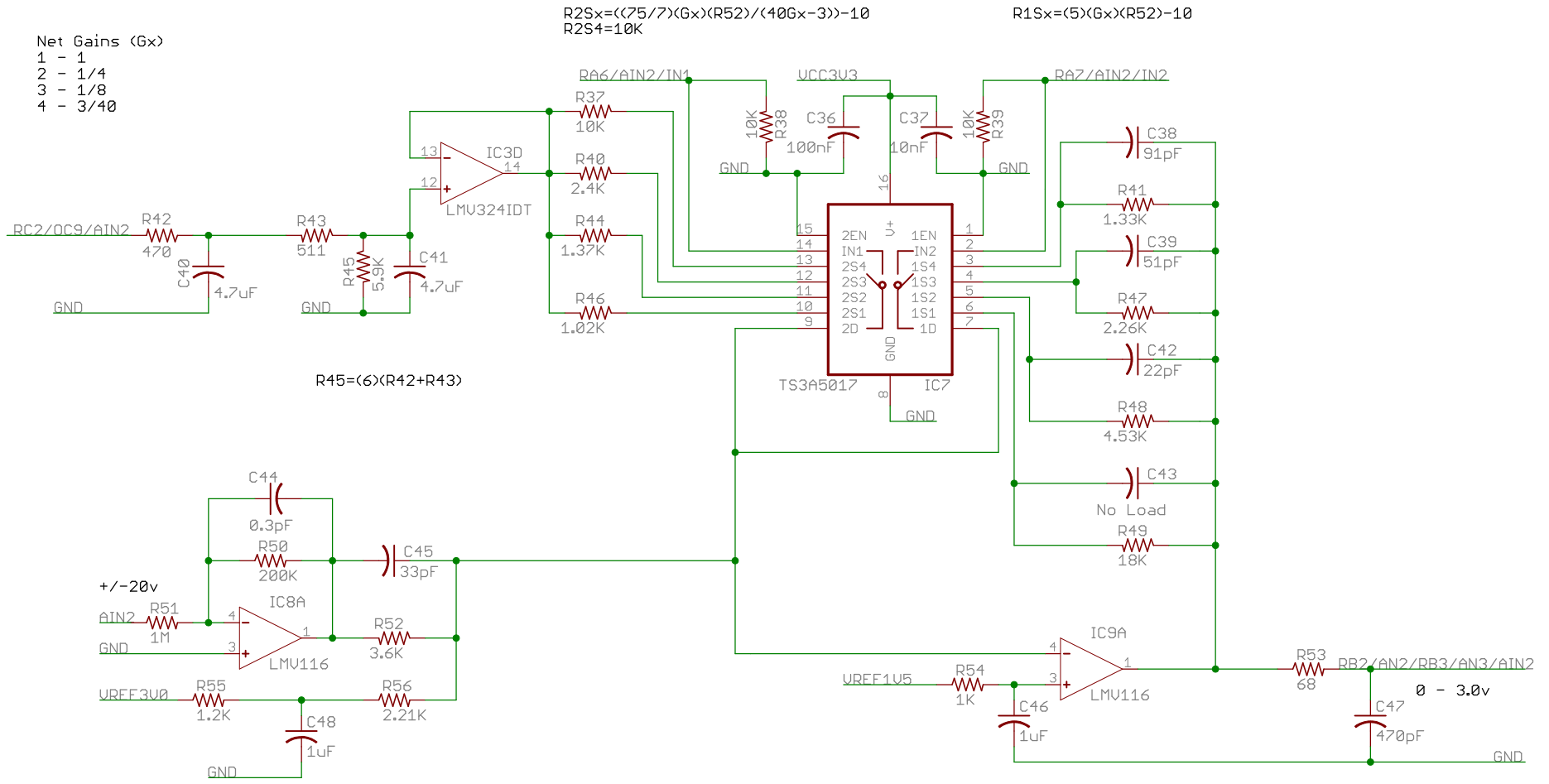
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Analog In Channel 1



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Analog In Channel 2

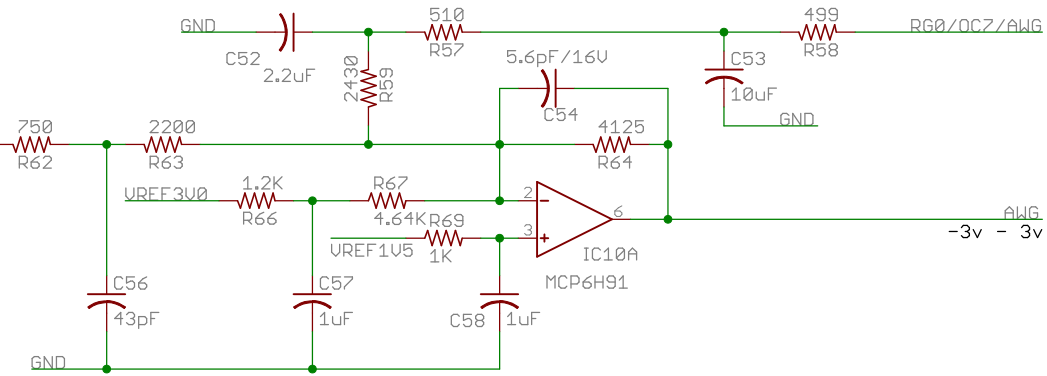
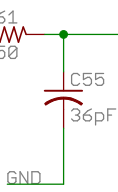
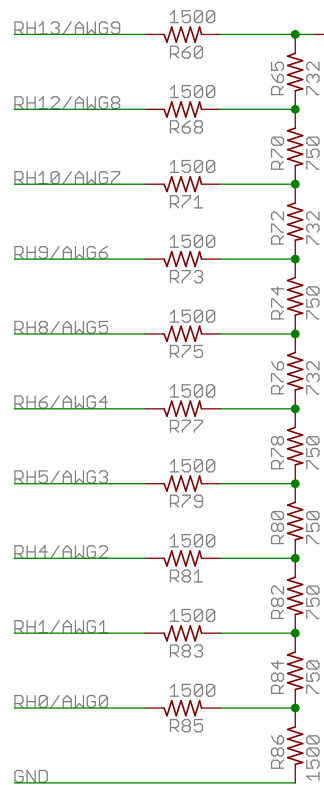


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R2R Ladder

Digital to Analog Converter

RL=1500
R65=R72=R76=(R84-2.5%)

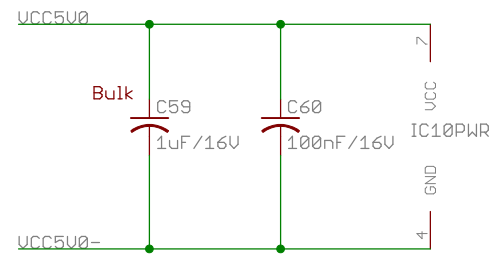


$$RLI = RL + R62 + R63 = 4450$$

$$R66 + R67 = (510 / 389) \times (RLI) = 5834$$

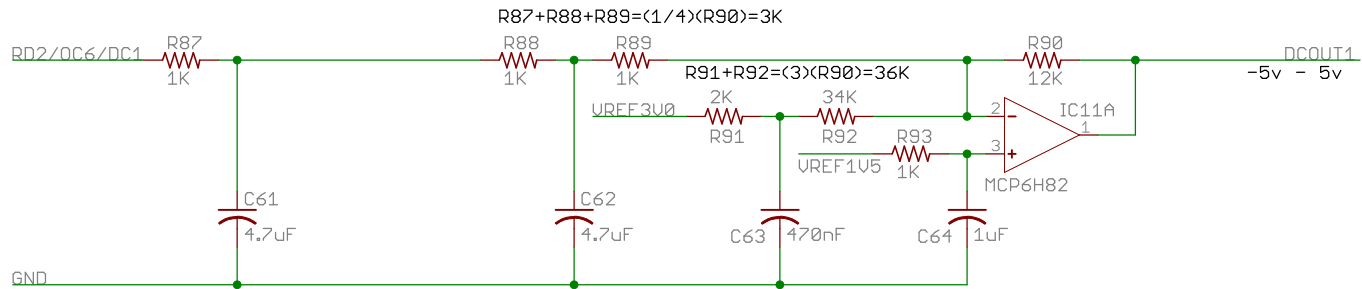
$$R57 + R58 + R59 = (17 / 22) \times (RLI) = 3439$$

$$R64 = (10 / 11) \times (RLI) + 2\% = (51 / 55) \times (RLI) = 4126$$

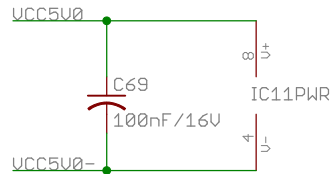
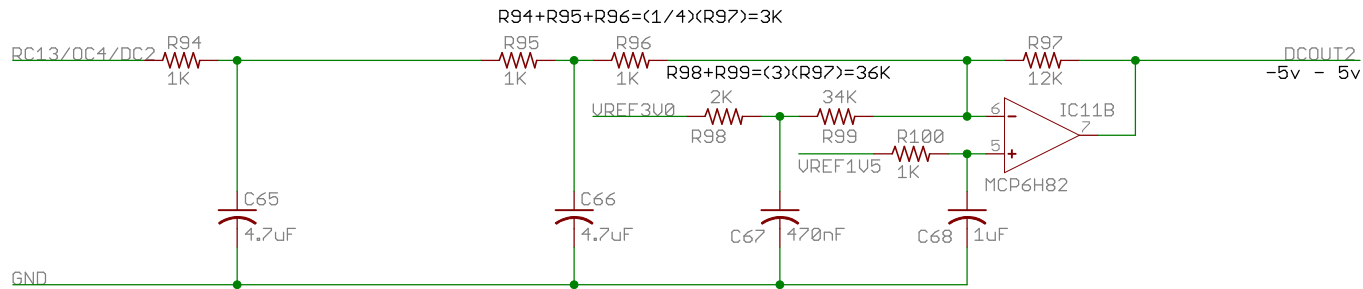


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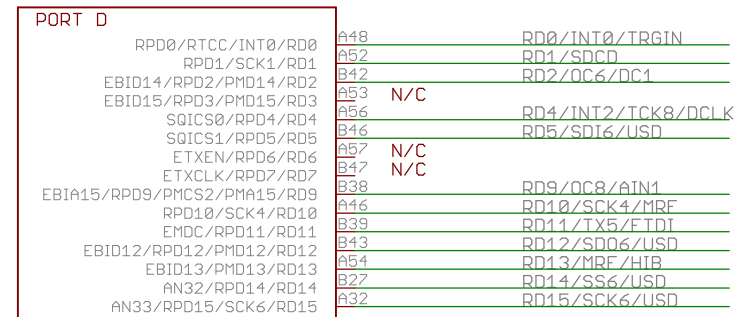
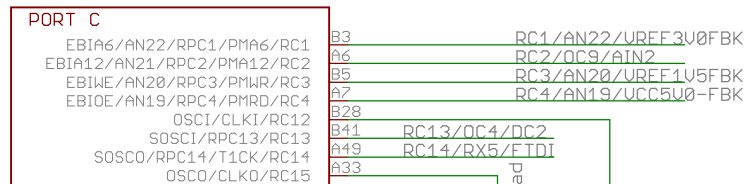
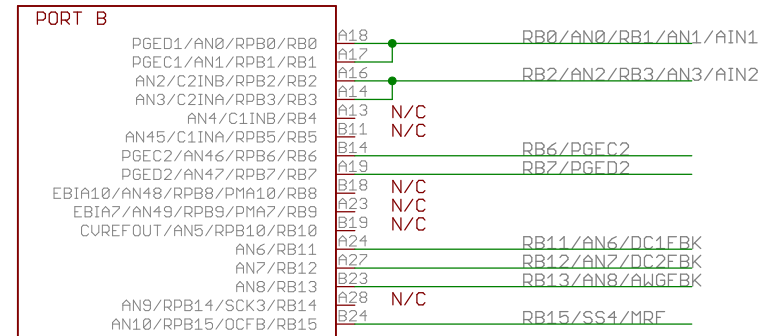
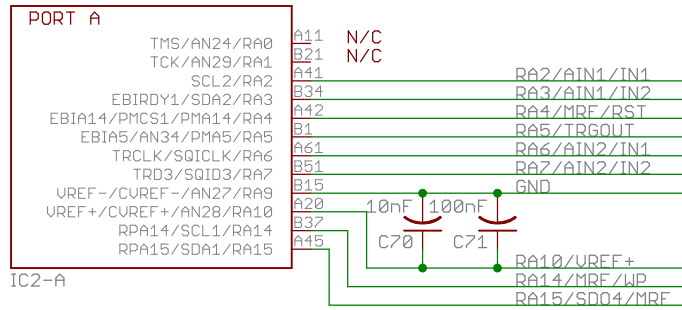
DC Output Channel 1



DC Output Channel 2



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PORT E		
EBID0/PMD0/RE0	B52	RF0/DI00
EBID1/PMD1/RE1	A64	RF1/DI01
EBID2/PMD2/RE2	A66	RF2/DI02
EBID3/RPE3/PMD3/RE3	B56	RF3/DI03
EBID4/AN18/PMD4/PE4	A67	RF4/DI04
EBID5/AN17/RPE5/PMD5/RE5	A3	RF5/DI05
EBID6/AN16/PMD6/RE6	B2	RF6/DI06
EBID7/AN15/PMD7/RE7	A4	RF7/DI07
AN25/RPE8/RE8	B10	RF8/DI08
AN26/RPE9/RE9	A12	RF9/DI09

IC2-E

PORT F		
EBID11/RPF0/PMD11/RF0	A59	RF0/SDI2/SDO2
EBID10/RPF1/PMD10/RF1	B49	RG6/SCK2/CTS1
SDA3/RPF2/RF2	B31	RF2/INT1/TCK9/PCLK
RPF3/USBID/RF3	A38	RF3/SS2/RIS1/OC2
EPIA9/RPF4/SDA5/PMA9/RF4	B36	RF4/SDA5/RX1/OC3
EPIA8/RPF5/SCL5/PMA8/RF5	A44	RF5/SDO2/SDI2/TX1/SCL5
SCL3/RPF8/RF8	A39	N/C
TDO/AN31/RPF12/RF12	B22	N/C
TDI/AN30/RPF13/SCK5/RF13	A26	N/C

IC2-F

PORT G		
EBID8/RPG0/PMD8/RG0	B50	RG0/OC7/AWG
EBID9/RPG1/PMD9/RG1	A60	N/C
AN14/C1IND/RPG6/SCK2/RG6	B6	RG6/SCK2/CTS1
AN13/C1INC/RPG7/SDA4/RG7	A8	RG7/SDI4/MRF
AN12/C2IND/RPG8/SCL4/RG8	B7	RG8/TINT3/MRF
EPIA2/AN11/C2INC/RPG9/PMA2/RG9	B9	RG9/AN11/UCC5V0FBK
TRD1/SQID1/RG12	A65	RG12/BTN_USER
TRD0/SQID0/RG13	B55	RF4/SDA5/RX1/OC3
TRD2/SQID2/RG14	B54	RF5/SDO2/SDI2/TX1/SCL5
AN23/RG15	A2	RG15/AN23/UCC3V3FBK

IC2-G

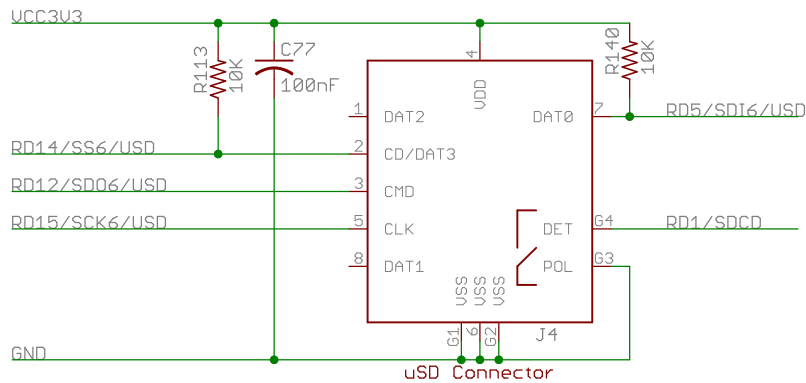
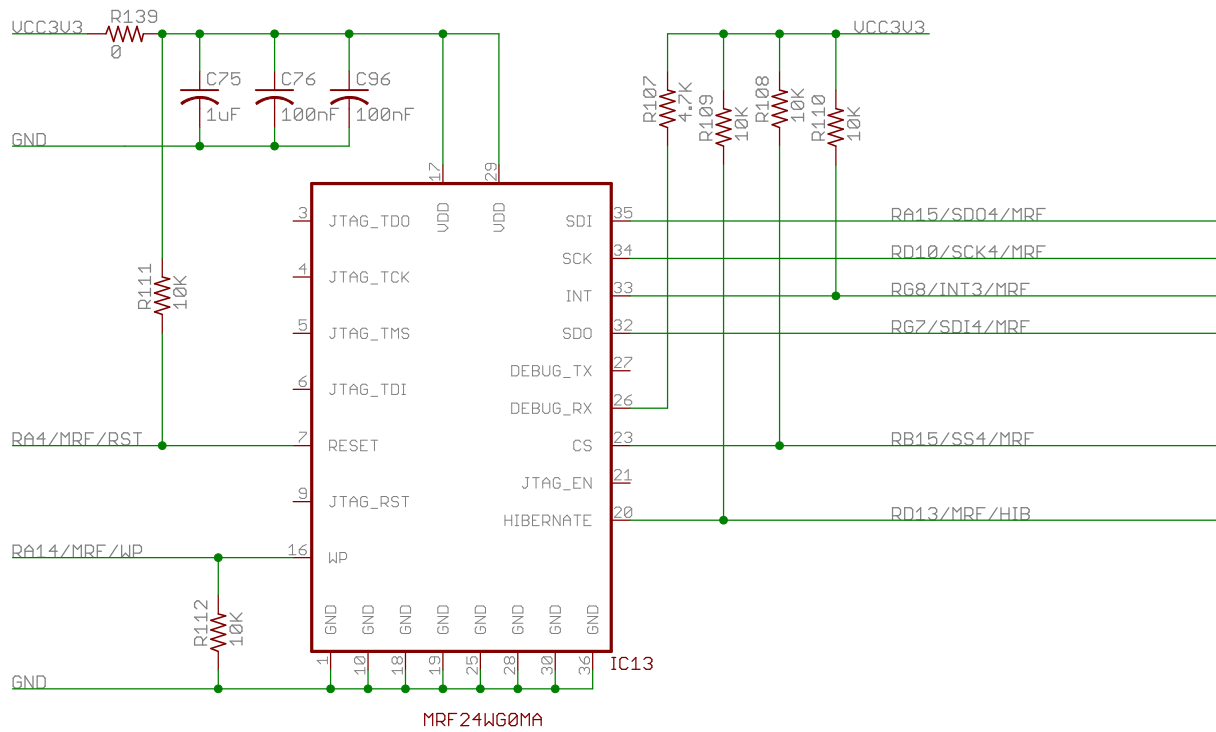
PORT H		
AN38/ETXD2/RH0	B17	RH0/AWG0
AN39/ETXD3/RH1	A22	RH1/AWG1
AN40/ERXERR/RH4	A30	RH4/AWG2
AN41/ERXD1/RH5	B26	RH5/AWG3
AN42/ERXD2/RH6	A31	RH6/AWG4
ERXD0/RH8	B32	RH8/AWG5
ERXD3/RH9	A40	RH9/AWG6
ECOL/RH10	B33	RH10/AWG7
ECRS/RH12	A47	RH12/AWG8
ERXDU/ECRSU/RH13	B40	RH13/AWG9

IC2-H

PORT J		
ETXERR/RJ0	B44	RJ0/LFD4
EMDIO/RJ1	A55	RJ1/LFD3
EBIRDY3/RJ2	B45	RJ2/LFD2
EBICS0/RJ4	A62	RJ4/LFD1
AN35/ETXD0/RJ8	A5	N/C
AN36/ETXD1/RJ9	B4	N/C
AN37/ERXCLK/EREFCLK/RJ11	B12	N/C

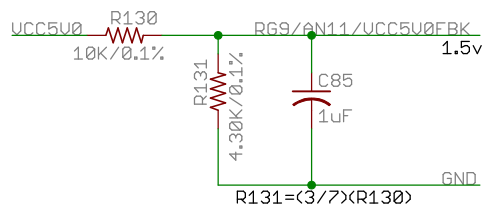
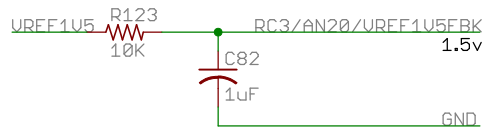
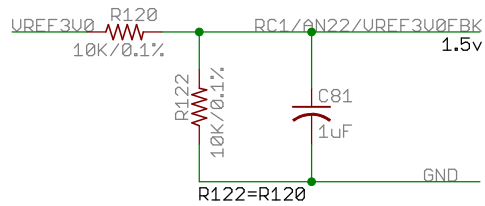
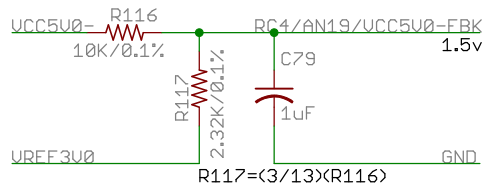
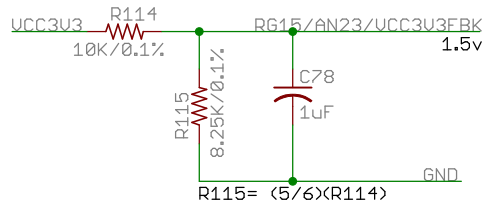
IC2-J

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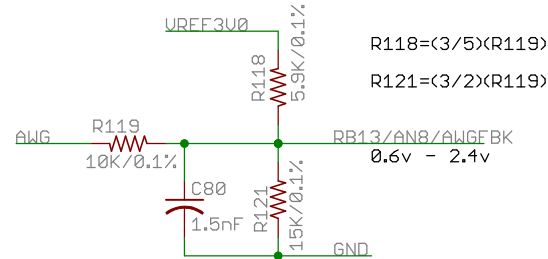


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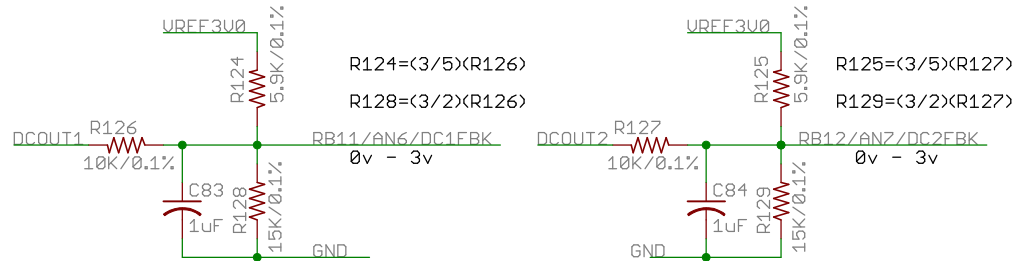
Power Feedback



Waveform Generator Feedback



Digital Output Feedback



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SHEET: Feedback Circuits

Author: GMA

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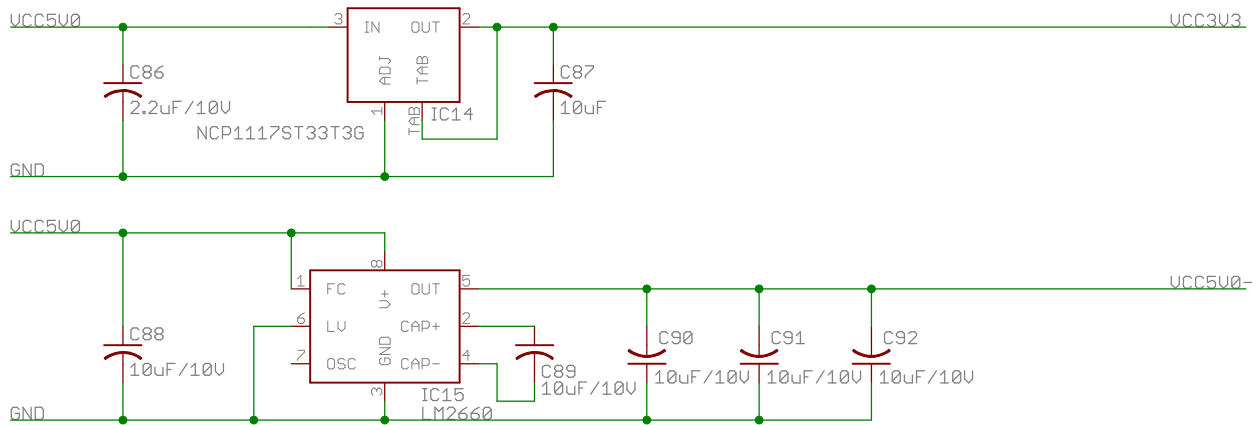
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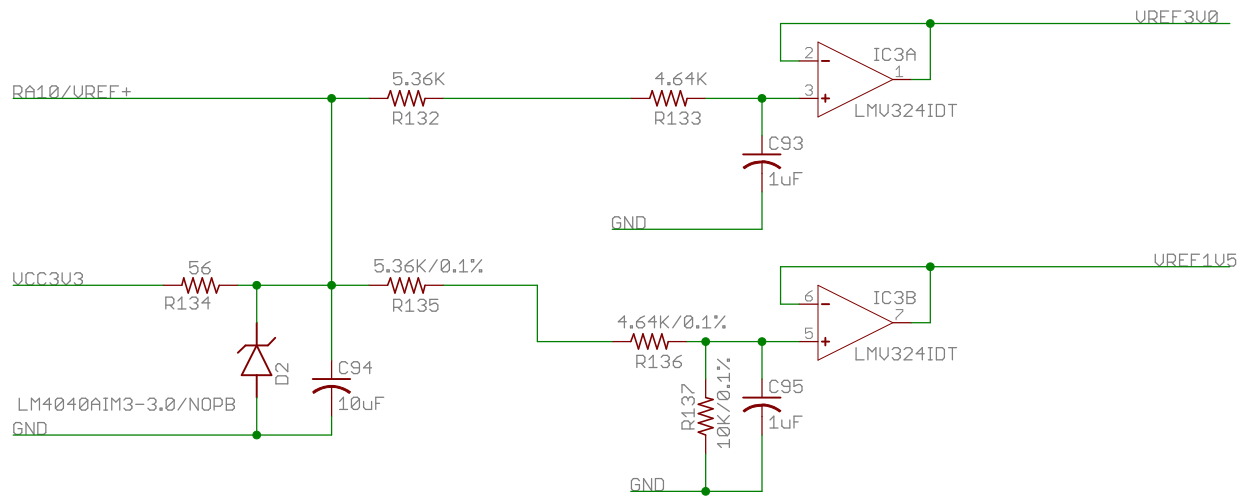
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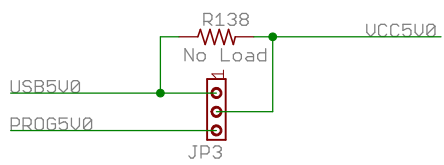
Regulators



Reference



Power Select



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