EE 660: Computer Architecture
Branch Prediction

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Based on the slides of Prof. David Wentzlaff
Agenda

• Branch Cost Motivation
• Branch Prediction
  – Outcome
    • Static
    • Dynamic
  – Target Address
Agenda

• Branch Cost Motivation

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Longer Frontends Means More Control Flow Penalty

Penalty includes instructions in IQ
Longer Pipeline Frontends Amplify Branch Cost

<table>
<thead>
<tr>
<th>Basic Pentium III Processor Misprediction Pipeline</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Fetch</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Basic Pentium 4 Processor Misprediction Pipeline</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 TC Nxt IP</td>
</tr>
</tbody>
</table>

Pentium 3: 10 cycle branch penalty
Pentium 4: 20 cycle branch penalty

Dual Issue and Branch Cost

PC

Instr. Cache

addr
rdata

IR0

IR1

RF Read

Branch Cond.

ALU A

ALU B

Data Cache

addr
rdata

RF Read
### Superscalars Multiply Branch Cost

<table>
<thead>
<tr>
<th>Instruction</th>
<th>F</th>
<th>D</th>
<th>I</th>
<th>A0</th>
<th>A1</th>
<th>W</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEQZ</td>
<td>F</td>
<td>D</td>
<td>I</td>
<td>A0</td>
<td>A1</td>
<td>W</td>
</tr>
<tr>
<td>OpA</td>
<td>F</td>
<td>D</td>
<td>I</td>
<td>B0</td>
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<td>OpB</td>
<td>F</td>
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<td>I</td>
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<tr>
<td>OpG</td>
<td>F</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>OpH</td>
<td>F</td>
<td>D</td>
<td>I</td>
<td>A0</td>
<td>A1</td>
<td>W</td>
</tr>
<tr>
<td>OpI</td>
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<td>D</td>
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<td>B0</td>
<td>B1</td>
<td>W</td>
</tr>
</tbody>
</table>

Dual-issue Processor has twice the mispredict penalty

How much work is lost if pipeline doesn’t follow correct instruction flow?

~pipeline width x branch penalty
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Branch Prediction

• Essential in modern processors to mitigate branch delay latencies

Two types of Prediction
1. Predict Branch Outcome
2. Predict Branch/Jump Address
Where is the Branch Information Known?

Know target address for branches, J, JAL

Know target address for JR, JALR

Know branch outcome
Agenda

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Branch Delay Slots
(expose control hazard to software)

• Change the ISA semantics so that the instruction that follows a jump or branch is always executed
  – gives compiler the flexibility to put in a useful instruction where normally a pipeline bubble would have resulted.

| I_1 | 096 | ADD |
| I_2 | 100 | BEQZ r1 +200 |
| I_3 | 104 | ADD |
| I_4 | 108 | ADD |
| I_5 | 304 | ADD |

Delay slot instructions executed regardless of branch outcome
Static Branch Prediction

Overall probability a branch is taken is \(~60\text{-}70\%\) but:

- **backward**: 90%
- **forward**: 50%
Static Software Branch Prediction

- Extend ISA to enable compiler to tell microarchitecture if branch is likely to be taken or not (Can be up to 80% accurate)

BR.T  F  D  X  M  W  
OpA     F   -   -   -  
Targ    F  D  X  M  W  
BR.N    F  D  X  M  W  
T       
OpB     F  D  X  M  W  
OpC     F  D  X  M  W  

What if hint is wrong?

BR.T  F  D  X  M  W  
OpA     F   -   -   -  
Targ    F   -   -   -  
OpA     F  D  X  M  W  

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Static Hardware Branch Prediction

1. Always Predict Not-Taken
   – What we have been assuming
   – Simple to implement
   – Know fall-through PC in Fetch
   – Poor Accuracy, especially on backward branches

2. Always Predict Taken
   – Difficult to implement because don’t know target until Decode
   – Poor accuracy on if-then-else

3. Backward Branch Taken, Forward Branch Not Taken
   – Better Accuracy
   – Difficult to implement because don’t know target until Decode
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Dynamic Hardware Branch Prediction: Exploiting Temporal Correlation

• Exploit structure in program: The way a branch resolves may be a good indicator of the way it will resolve the next time it executes (Temporal Correlation)

1-bit Saturating Counter

Diagram:

- Predict T
- Predict NT
- NT
- T
- T
- NT
1-bit Saturating Counter

For Backward branch in loop
• Assume 4 Iterations
• Assume is executed multiple times

Always 2 Mispredicts
2-bit Saturating Counter

<table>
<thead>
<tr>
<th>Iteration</th>
<th>Prediction</th>
<th>Actual</th>
<th>Mispredict?</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NT</td>
<td>T</td>
<td>Y</td>
<td>Strong NT</td>
</tr>
<tr>
<td>2</td>
<td>NT</td>
<td>T</td>
<td>Y</td>
<td>Weak NT</td>
</tr>
<tr>
<td>3</td>
<td>T</td>
<td>T</td>
<td></td>
<td>Weak T</td>
</tr>
<tr>
<td>4</td>
<td>T</td>
<td>NT</td>
<td>Y</td>
<td>Strong T</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>T</td>
<td>T</td>
<td></td>
<td>Weak T</td>
</tr>
<tr>
<td>2</td>
<td>T</td>
<td>T</td>
<td></td>
<td>Strong T</td>
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<tr>
<td>3</td>
<td>T</td>
<td>T</td>
<td></td>
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<td>4</td>
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<td>NT</td>
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</table>

Only 1 Mispredict
Other 2-bit FSM Branch Predictors

Jump directly to strong from weak

Weak Taken

Strong Not Taken

Weak Not Taken

Strong Taken
Branch History Table (BHT)

4K-entry BHT, 2 bits/entry, ~80-90% correct predictions
Exploiting Spatial Correlation

Yeh and Patt, 1992

```latex
\begin{verbatim}
if (x[i] < 7) then
  y += 1;
if (x[i] < 5) then
  c -= 4;
\end{verbatim}
```

If first condition false, second condition also false

**Branch History Register**, BHR, records the direction of the last N branches executed by the processor (Shift Register)
Pattern History Table (PHT)
Two-Level Branch Predictor

Branch Outcome (T/NT) → BHR → Indexes PHT → PHT 0 → ... → PHT $2^{(k-1)}$ → FSM Output Logic → Prediction (T/NT)

PC → k
Generalized Two-Level Branch Predictor

For non-trivial m and k, > 97% accuracy
Tournament Predictors (ex: Alpha 21264)

- Choice predictor learns whether best to use local or global branch history in predicting next branch
- Global history is speculatively updated but restored on mispredict
- Claim 90-100% success on range of applications
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Even with best possible prediction of branch outcome, still have to wait for branch target address to be determined
Branch Target Buffer (BTB)

Put BTB in Fetch Stage in parallel with PC+4 Speculation logic
BTB is only for Control Instructions

- BTB contains useful information for branch and jump instructions only
  - Do not update it for other instructions

- For all other instructions the next PC is PC+4!

*How to achieve this effect without decoding the instruction?*

*When do we update BTB information?*
Uses of Jump Register (JR)

- Switch statements (jump to address of matching case)
  BTB works well if same case used repeatedly

- Dynamic function call (jump to run-time function address)
  BTB works well if same function usually called, (e.g., in C++ programming, when objects have same type in virtual function call)

- Subroutine returns (jump to return address)
  BTB works well if usually return to the same place

  ⇒ Often one function called from many distinct call

How well does BTB work for each of these cases?
Subroutine Return Stack

Small structure to accelerate JR for subroutine returns, typically much more accurate than BTBs.

```c
fa() { fb(); }
fb() { fc(); }
fcc() { fd(); }
```

Push call address when function call executed

Pop return address when subroutine return decoded

\[
\begin{align*}
&\text{&fd()} \\
&\text{&fc()} \\
&\text{&fb()}
\end{align*}
\]

k entries
(typically k=8-16)
Acknowledgements

• These slides contain material developed and copyright by:
  – Arvind (MIT)
  – Krste Asanovic (MIT/UCB)
  – Joel Emer (Intel/MIT)
  – James Hoe (CMU)
  – John Kubiatowicz (UCB)
  – David Patterson (UCB)
  – Christopher Batten (Cornell)

• MIT material derived from course 6.823
• UCB material derived from course CS252 & CS152
• Cornell material derived from course ECE 4750