Foundations of Analog and Digital Electronic Circuits

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Chapter 15

The Operational Amplifier Abstraction

15.1 Introduction

This chapter introduces a very powerful amplifier abstraction called the *Operational Amplifier* or *Op Amp*. Much as the gate abstraction forms the foundation of most of digital electronics, the operational amplifier forms the basis for much of electronic circuit design.

The Op Amp is a multistage two-input differential amplifier that is designed to be an almost ideal control device, specifically, a voltage controlled voltage source. An abstract representation of the operational amplifier shown in Figure 15.1 suggests it is a four-port device. The four ports are an input port, an output port and a pair of power ports. A $+V_S$ voltage (for example, 15 volts) is applied at the plus power port and a $-V_S$ voltage (for example, -15 volts) is applied at the minus power port. An input voltage (the control) applied across the non-inverting and inverting input terminals of the Op Amp is amplified by a large amount and appears at the output port. In the operational amplifier abstraction, the input impedance across the input port is infinity, and the output impedance is zero. The gain, or the factor by which the input voltage is amplified, is also infinity.

This chapter uses the Op Amp to construct more complex circuits using its simple, abstract model. Internally, the Op Amp itself is a moderately complicated circuit (see, for example, Figure 15.2) and its design is beyond the scope of this book. Briefly, it contains an input stage not unlike the differential amplifier discussed in Example 7.21 in Chapter 7, or Example 8.3 in Chapter 8. This differential input stage gives the Op Amp its high input resistance, and a high gain. It also converts the differential input

CHAPTER 15. THE OPERATIONAL AMPLIFIER ABSTRACTION

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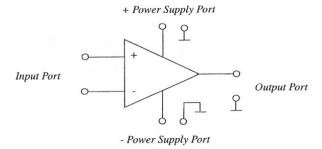


Figure 15.1: The Operational Amplifier Abstraction

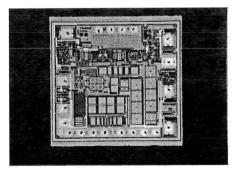


Figure 15.2: A chip photograph of the MAX406 Op Amp from Maxim. The chip is roughly 2mm on a side

voltage to a single-ended output. ¹ Typical Op Amps also have a second stage similar to the second stage in Example 7.21 in Chapter 7, which provides additional amplification and level shifts the output voltage to zero when both inputs are equal. Op Amps may also have an output stage similar to the buffer illustrated in Figure 8.40 in Chapter 8, which gives the Op Amp its low output impedance.

In this chapter, initially, our discussion will be in terms of circuits containing Op Amps and resistors. After the basic ideas of Op Amps used as dependent sources and negative feedback have become familiar, circuits with both capacitors and resistors will be introduced.

¹Op Amps with single-ended inputs are also useful. Example 15.1 discusses one such.

15.1.1 Historical Perspective

The name "operational amplifier" originates from the bygone days of the analog computer (1940-1960), in which the constants in differential equations were represented by the gains of amplifiers. Thus these amplifiers, constructed from balanced pairs of specially manufactured vacuum tubes, had to have reliable, known, fixed gains. Because transistors are inherently more temperature-dependent than vacuum tubes, it was at first thought that satisfactory transistor Op Amps could not be built. But in 1964 it was discovered that by fabricating balanced transistor pairs close together on a single silicon chip to minimize thermal gradients, the temperature problems could be overcome. And thus were born in rapid succession the 703, the 709, and then the ubiquitous 741. Op Amps are rarely used for analog computers any more, but instead have become universal building blocks in all aspects of analog circuitry.

15.2 Device Properties of the Operational Amplifier

The symbol and standard labeling for the operational amplifier are shown in Figure 15.3a. The two required external power supplies have been explicitly shown in the diagram, although showing them is not the usual practice. All five currents have been labeled, in addition to appropriate node voltages, referred to the indicated common ground terminal. In this primitive circuit, the voltage v_i is used to control the output voltage v_o . Let us examine this control function in detail to find out both the extent of the control, and the cost of the control, that is, how much power must be applied from source v_i to control a given amount of power at the v_o terminal. To address the first problem, we set up the circuit exactly as in Figure 15.3, and measure the output voltage v_o , both as a function of time and as a function of v_i , assuming v_i is some low frequency sinusoid. The results are shown in Figure 15.3b and c. Note the difference in scale of the voltage axes, indicating that the output voltage is perhaps 300,000 times as large as the input voltage. The plot of v_o versus v_i shows a region around the origin where v_o is fairly linearly related to v_i , but much beyond this range the control becomes ineffective, and v_o stays at a fixed voltage, or saturates, at roughly either +12 volts or -12 volts, depending on the polarity of v_i . The curves will also differ for different samples of the same Op Amp type.

Separate measurements on the device, not illustrated in Figure 15.3, would indicate that the maximum output current i_o is about 10 mA for the 741, and that the input currents i^- and i^+ are extremely small, of the order of 10^{-7} amps. Thus it is obvious without any formal calculation that the amount of input power required for the control function is orders of magnitude smaller than the power which can be controlled at the output.

The curve of output voltage versus input voltage, Figure 15.3c, is nonlinear. But

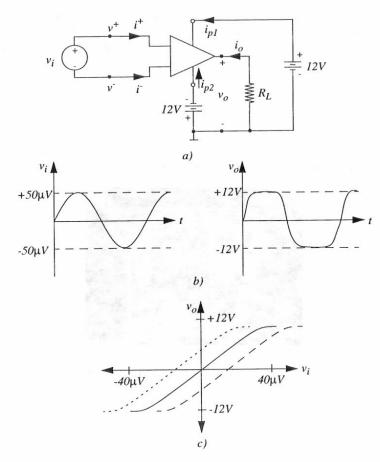


Figure 15.3: Operational amplifier characteristic. As illustrated by the dashed lines in (c), different devices of the same type might have different characteristics. The characteristics might also depend on temperature

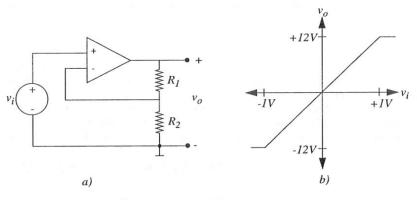


Figure 15.4: Non-inverting Op Amp amplifier. The characteristic in (b) assumes $R_1/R_2=11$

we also observe that the device has very large voltage gain, defined as $\Delta v_o/\Delta v_i$. We certainly would be willing to sacrifice substantial amounts of gain in return for a corresponding improvement in linearity. Fortunately, the addition of two resistors to the circuit results in precisely this trade-off. Figure 15.4 shows one possible circuit configuration, and the resulting relation between v_o and v_i . We will have more to say about this circuit in Section 15.3.1.

15.2.1 The Op Amp Model

To gain some insight about how the circuit in Figure 15.4 is working, we first need a circuit model which approximates the Op Amp behavior illustrated in the data in Figure 15.3. On the basis of the preceding chapters, we are led to assign node voltages as in Figure 15.3a, and apply KCL to the circuit. The current law equation turns out to be not very helpful, but it is important to understand why, so we proceed. From Figure 15.3a,

$$i^{+} + i^{-} + i_{p1} + i_{p2} + i_{o} = 0 (15.1)$$

As noted above, i^+ and i^- are about four orders of magnitude smaller than i_o hence

$$i_o \simeq -i_{p1} - i_{p2}$$
 (15.2)

But i_{p1} and i_{p2} are both power supply currents, so Equation 15.2 merely states that the output current comes from the power supplies. Important, but not very useful

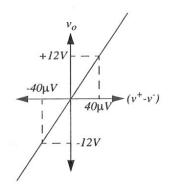


Figure 15.5: Linearized characteristic

(except possibly for the calculation of power dissipation).

Figure 15.3c offers more insight. We see that in the center of the characteristic, the output voltage is approximately proportional to the input voltage, or, more precisely, to the difference between v^+ and v^- . (Note that v^+ and v^- are *labels* for voltages, and hence each can be positive or negative, depending on the circuit.) If we idealize this relationship by making it linear, then the curve of Figure 15.5 results. The curve can now be expressed mathematically as

$$v_o = A(v^+ - v^-) (15.3)$$

This is the mathematical representation of a *voltage-dependent voltage source*, controlled by $(v^+ - v^-)$. For this particular device the constant A, the voltage gain, is 300,000.

The model in Figure 15.6 represents Equation 15.3 in circuit terms. To clearly distinguish the dependent source from an independent source, as before, all dependent sources are represented by diamond-shaped symbols. The disembodied wires on the left of the diagram are distressing at first sight, but merely indicate that the input current to this ideal voltage-controlled voltage source is zero by definition; i.e., $i^+ = i^- = 0$.

The dependent source of Figure 15.6 by itself is clearly an imperfect model of an Op Amp. The saturation so clearly present in Figure 15.3c is missing from Figure 15.5 and from the model of Figure 15.6, as is the temperature dependence. To simplify the initial discussion, we shall ignore saturation effects in Op Amps when discussing linear circuits by assuming that we always operate in the central linear part of the amplifier characteristic. We will specifically examine saturation behavior of Op Amps in Section 15.7.

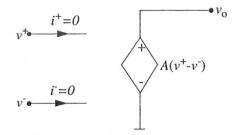


Figure 15.6: Voltage-controlled voltage source

As a summary, the idealized Op Amp model shown in Figure 15.6 has the following properties:

• The output voltage

$$v_o = A(v^+ - v^-)$$

where the gain $A \to \infty$. The output resistance is 0.

• The input currents $i^+ = 0$ and $i^- = 0$. Accordingly, the input resistance is infinite.

15.3 Simple Op Amp Circuits

15.3.1 The Non-inverting Op Amp

Now we are in a position to find an analytical relation between v_o and v_i for the circuit in Figure 15.4. We replace the Op Amp by the linear model in Figure 15.6, as shown in Figure 15.7, then analyze this linear circuit by the methods of Chapter 3. The voltage variables defined in the figure are in fact the node variables for the circuit, so we can use the node method to derive three independent expressions relating the three unknown voltages.

First, notice that

$$v^+ = v_i \tag{15.4}$$

since v_i is the branch voltage between v^+ and the ground node.

Next, recalling that the model specifically assumes no input current, that is, $i^- \simeq 0$,

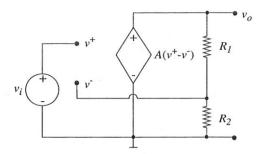


Figure 15.7: Model of a non-inverting Op Amp amplifier

we write the node equation at the node with voltage v^- as

$$\frac{v^-}{R_2} + \frac{v^- - v_o}{R_1} = 0$$

Or,

$$v^{-} = \frac{R_2}{R_1 + R_2} v_o \tag{15.5}$$

The dependent-source relation yields our third equation

$$v_0 = A(v^+ - v^-) (15.6)$$

Substituting and solving, we obtain

$$v_o = \frac{Av_i}{1 + A\frac{R_2}{R_1 + R_2}} \tag{15.7}$$

Recall that A is very large, 300,000 in our case, so if the voltage divider does not introduce too much attenuation,

$$\frac{AR_2}{R_1 + R_2} >> 1 \tag{15.8}$$

hence we can neglect the "1" term in the denominator of Equation 15.7 to obtain the approximate result

$$v_o \simeq \frac{R_1 + R_2}{R_2} v_i \tag{15.9}$$

This is an important result. It says that the relation between v_o and v_i , is almost independent of the somewhat unreliable gain constant A of the original Op Amp.

In other words, because resistor values are stable, reliable and very insensitive to temperature, we expect v_o in this circuit to be a stable reliable function of v_i . But this reliability has come at a price: the gain is now much less than for the Op Amp alone somewhere between 1 and 1,000 depending on the choice of R_1 and R_2 (but not more than 1000, or the inequality, Equation 15.8, will no longer be valid).

Several important conclusions can be drawn from this simple example.

- It is possible to construct from a high-gain Op Amp and a pair of resistors a reliable amplifier with a known fixed gain. This particular configuration is called the non-inverting connection.
- Negative feedback:

The basic structure of this circuit, in which some of the output signal is brought back to the input of the circuit, and compared with the input signal, is called negative feedback.

For the feedback to be negative in simple Op Amp circuits, the attenuated output signal must be fed back to the v^- terminal. If the output signal is fed back only to the v^+ input, very different behavior results, as we shall see. The first-order consequences of these connections will be explored in this chapter, but more complex issues of stability and oscillations are dealt with in books on Signals and Systems.

- We have chosen to model the Op Amp by the dependent source of Figure 15.6, which is a voltage-controlled voltage source, for obvious reasons.
- Although the +12 volt and -12 volt DC power supplies are obviously necessary
 for Op Amp operation, (they power the voltage-controlled voltage source), their
 inclusion in the circuit model we use for analysis is not very helpful, because
 the KCL calculation does not yield a useful relation. Calculating the current
 through a voltage source rarely provides useful insight, because a voltage source
 can support any current.

The use of feedback as a way of building stable reliable systems is so intertwined with our daily lives that we are totally unaware of it. Familiar examples are household furnace controls, and "cruise controls" and "anti-lock brakes" on automobiles.

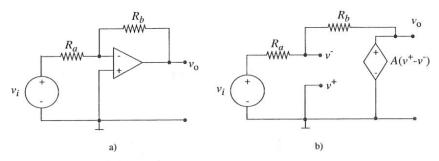


Figure 15.8: Inverting Op Amp

15.3.2 A Second Example: The Inverting Connection

Another very common Op Amp circuit, the "inverting connection", is shown in Figure 15.8a. For negative feedback, the signal from the output must find its way to the *negative* terminal of the Op Amp as shown.

If we use the Op Amp model in Figure 15.6, hereafter referred to as the *ideal Op Amp model*, then the circuit model for the inverting amplifier is as shown in Figure 15.8b. Following the same analysis method as before, we will derive three independent equations relating the three unknown node voltages v^+ , v^- , and v_o . Accordingly, by inspection

$$v^{+} = 0$$

Summing the currents at the v^- node, we find, assuming the v^- terminal of the Op Amp draws no current

 $\frac{(v_i - v^-)}{R_o} + \frac{(v_o - v^-)}{R_b} = 0 {(15.10)}$

Hence

$$v^- = \frac{R_b}{R_a + R_b} v_i + \frac{R_a}{R_a + R_b} v_o$$

The Op Amp output relation yields

$$v_o = A(v^+ - v^-) (15.11)$$

Substituting and solving, we obtain

$$v_o = \frac{-AR_b/(R_a + R_b)}{1 + AR_a/(R_a + R_b)}v_i$$
 (15.12)

As before, if we assume A is of the order of 10^5 , and the resistor ratio $R_a/(R_a+R_b)$ is not less than 0.001, then

$$A\frac{R_a}{R_a + R_b} >> 1 \tag{15.13}$$

and Equation 15.12 can be approximated as

$$v_o \simeq -\frac{R_b}{R_a} v_i \tag{15.14}$$

Again we have a relation between the input and the output voltage that is almost independent of the unreliable gain A, and dependent only on resistor ratios. But this time the output signal is *inverted* compared to the input signal, as indicated by the minus sign. Equation 15.14 for the inverting connection and the corresponding equation for the non-inverting case, Equation 15.9, are encountered so frequently that they rapidly become primitives in our circuit analysis repertoire, as with the voltage divider and current divider relations.

One might be tempted to use superposition on v_i and the dependent source $A(v^+ - v^-)$ in Figure 15.8b to find v^- , but as discussed in Section 3.5.1 this is a hazardous approach. The problem is that the value of the dependent source is controlled by some other variable in the circuit, so we are not free to simply set the source to zero.

The safest rule to follow is: do *not* set dependent sources to zero in superposition calculations.

Example 15.1 Single Ended Amplifier

Circuits containing single-input amplifiers can be analyzed in much the same way as circuits containing Op Amps, as this example shows. Consider the circuit shown in Figure 15.9, which contains a single-input inverting amplifier having gain -A. Except for its finite gain, the amplifier is assumed to be ideal. Thus, its input current is zero, it drives $v_{OUT} = -Av_{MID}$, and its negative feedback makes the circuit stable.

Following the node method,

$$0 = \frac{v_{MID} - v_{IN}}{R_1} + \frac{v_{MID} - v_{OUT}}{R_2}$$

with

$$v_{OUT} = -Av_{MID}$$
 .

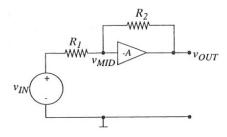


Figure 15.9: A single ended amplifier in a feeback loop. Note that power supply and ground connections to the Op Amp are not shown

Combining these two equations yields

$$v_{OUT} = \frac{-A(R_2/R_1)}{A+1+(R_2/R_1)}v_{IN} \quad ,$$

which is identical to the result obtained for the inverting amplifier constructed with an Op Amp. For example, with $R_1=1~\mathrm{k}\Omega,~R_2=100~\mathrm{k}\Omega$ and $A=10^5,~v_{OUT}=99.9v_{IN}.$

Further, in the limit $A \to \infty$,

$$v_{OUT} = -\frac{R_2}{R_1} v_{IN}$$

15.3.3 Sensitivity

It is helpful at this point to be more precise about just how "independent" v_o really is to changes in the Op Amp gain A. Let G be the gain v_o/v_i of the Op Amp circuit. Then for the non-inverting connection, for example, we find from Equation 15.7

$$G = \frac{v_o}{v_i} = \frac{A}{1 + A\frac{R_2}{R_1 + R_2}} \tag{15.15}$$

Taking the differential, assuming small changes in A and constant R_1 and R_2 , we obtain

$$dG = \frac{1}{(1 + A\frac{R_2}{R_1 + R_2})^2} dA \tag{15.16}$$

The fractional change in circuit gain is then, from Equation 15.15,

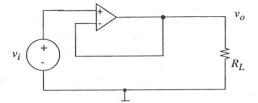


Figure 15.10: Follower

$$\frac{dG}{G} = \left(\frac{1}{1 + A\frac{R_2}{R_1 + R_2}}\right) \frac{dA}{A} \tag{15.17}$$

Thus with negative feedback a given percentage change in the Op Amp gain A results in a much smaller percentage change in the overall circuit gain G, smaller by a factor $1 + AR_2/(R_1 + R_2)$. Note from Equation 15.7 that this is exactly the factor by which the gain is reduced as a result of applying the feedback. By inspection of Figure 15.7, the gain term $AR_2/(R_1 + R_2)$ represents the gain for a signal traveling all the way around the feedback loop: through the Op Amp with its gain of A, then through the feedback resistor network with a "gain" of $R_2/(R_1 + R_2)$, (hence called the loop gain). In general, for negative feedback, gain changes are suppressed by a factor 1 + (loop gain), and the overall gain is reduced by this same factor.

15.3.4 A Special Case: The Voltage Follower

A useful circuit for isolating one electrical system from another is the *voltage follower* shown in Figure 15.10. Comparison with Figure 15.4a indicates that this circuit is a degenerate case of the non-inverting connection, in which $R_1=0$ and $R_2=\infty$. Hence, from Equation 15.9, the input-output relation for the follower is

$$v_o \simeq v_i \tag{15.18}$$

That is, within a part of 10^{-5} or so, the output voltage is equal to the input voltage. An obvious question: why not just use a piece of copper wire to get the gain of one in Equation 15.18? To answer, we need only look at the currents. The current that must be supplied by the input source is i^+ , hence is a few nanoamps. The maximum current that can be supplied to some load by the Op Amp output circuit is a few milliamperes. Thus for a one-volt signal level, the circuit is drawing perhaps 10^{-8} watts from the

signal source, but can deliver 10^{-3} watts to the load resistor R_L . A piece of wire obviously produces no such power gain. Said in another way, the Op Amp is providing isolation between the input and the output parts of the circuit, in the sense that the output resistor R_L can be changed by many orders of magnitude, with a corresponding orders of magnitude change in output current, but the output voltage and the input current will be virtually unchanged. This isolation is referred to as buffering.

15.3.5 An Additional Constraint: $v^+ - v^- \simeq 0$

In all preceding Op Amp calculations, we have made an approximation that because the so-called loop gain in the denominator is much bigger than one, the "one" term can be neglected. This approximation is almost always valid in Op Amp calculations. It is the factor 1+ (loop gain) that determines how insensitive the circuit is to changes in the Op Amp gain constant A (see Equation 15.17, for example), hence large loop gain is clearly a desirable design goal. If the loop gain is almost always going to be large, it seems a bit clumsy (although clearly correct) to make the circuit calculations without taking this fact into account until the last line. One would hope that with some hindsight, it might be possible to make the "large loop gain" assumption at the start of the circuit calculation, thereby simplifying the math. Let us re-examine the circuit of Figure 15.8b with this in mind.

We know that for most Op Amps, A will be 100,000 or larger, and the maximum allowed v_o will be about 12 volts (see Figure 15.3c). Hence the largest value of $(v^+ - v^-)$ for linear operation will be around 120 microvolts, a voltage orders of magnitude smaller than either the input or the output voltage. On this basis it is reasonable to assume, as before, $i^+ \simeq 0$, and $i^- \simeq 0$, but include an additional constraint

$$v^{+} - v^{-} \simeq 0 \tag{15.19}$$

Not equal to zero, just small compared to other circuit voltages. When these three constraints are applied to the circuit in Fig 15.8b, we find

$$p^+ = 0$$

 $p^- \simeq 0$

Hence KCL at the v^- node yields

$$\frac{v_i}{R_o} + \frac{v_o}{R_b} \simeq 0 \tag{15.20}$$

(compare with Equation 15.10). Solving for v_o , we find

$$v_o \simeq -\frac{R_b}{R_a} v_i \tag{15.21}$$

as before, except this time the calculation is much simpler, because the combined constraints of approximately zero voltage and approximately zero current are quite powerful. For the non-inverting circuit of Figure 15.7, for example, we can write, using the voltage divider relation,

$$v_i = v^+ \simeq v^- = \frac{R_2}{R_1 + R_2} v_o$$
 (15.22)

Hence

$$v_o \simeq \frac{R_1 + R_2}{R_2} v_i \tag{15.23}$$

as before. The voltage constraint of Equation 15.19 is also called the *virtual ground constraint*², and can be interpreted in physical terms by noting that the output of a circuit with negative feedback must adjust itself to *force* $(v^+ - v^-)$ to be nearly zero, because that nearly-zero voltage is in turn multiplied by 100,000 to become the output voltage.

Note: The $v^+ - v^- \simeq 0$ constraint can only be applied if the Op Amp is not saturated and the feedback is negative, that is, the net feedback signal comes from the output back to the negative input terminal.

15.4 Input and Output Resistances

15.4.1 Output Resistance, Inverting Op Amp

Negative feedback has a profound effect on the Thévenin-equivalent input and output resistances of circuits. To illustrate, we calculate first the Thévenin output resistance of the simple inverting Op Amp assumed to be operating in the active (non-saturated) region, that is, the circuit in Figure 15.8b. Obviously if we model the Op Amp by the ideal Op Amp model, the Thévenin output resistance is by definition zero, with or without feedback. So to show any effect, we must use a more accurate device model which includes some finite resistance in series with the dependent source, as in Figure 15.11. One way of calculating the Thévenin output resistance is to apply a test current i_t , at the output terminals, as shown in the figure, and calculate the resulting voltage v_t , when all other *independent sources*, in this case v_i , are set to zero.

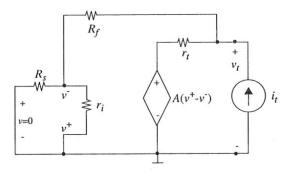


Figure 15.11: Calculation of output resistance

Note: In calculating the Thévenin resistance do **not** casually set dependent sources to zero, as their value is dictated by some other variable in the circuit which may or may not be zero.

The calculation of v_t is straightforward. We use the node method with conductances in place of resistances for convenience. In other words, we use $g_i=1/r_i$, $G_s=1/R_s$, $G_f=1/R_f$, and $g_t=1/r_t$. Applying KCL at the nodes with unknown node voltages, we get the following three independent equations

$$v^+ = 0 (15.24)$$

$$v^{-} = \frac{G_f}{G_f + G_s + g_i} v_t \qquad (15.25)$$

$$i_t + [A(v^+ - v^-) - v_t]g_t + (v^- - v_t)G_f = 0 (15.26)$$

(15.27)

To simplify the mathematics, we now assume for this calculation that r_i is infinite $(g_i = 0)$, because it is always much larger than R_s or R_f . Now, eliminating v^+ and v^- from Equation 15.26,

$$\frac{i_t}{v_t} = G_o = \frac{AG_f g_t}{G_f + G_s} + g_t + \frac{G_f G_s}{G_f + G_s}$$
(15.28)

Thus the output conductance is the sum of three conductances. The first term is the effect of the feedback, the second term is the output conductance of the Op Amp alone, and the third term in resistance notation is $R_f + R_s$, hence is the effect of the feedback resistors in the absence of the Op Amp. For large A, this last term is not important, so the Thévenin output conductance with feedback is

²Or more accurately, the *virtual short constraint*, since the inverting and non-inverting inputs need not always be at ground potential.

$$\frac{i_t}{v_t} = G_o \simeq g_t \left[1 + \frac{AG_f}{G_f + G_s} \right] \tag{15.29}$$

or, in more familiar terms

$$G_o \simeq g_t \left[1 + A \frac{R_s}{R_s + R_f} \right] \tag{15.30}$$

Hence the Thévenin output resistance of the circuit is

$$R_o \simeq \frac{r_t}{1 + A \frac{R_s}{R_s + R_t}}$$
 (15.31)

For large loop gain

$$R_o \simeq \frac{r_t}{A_{\frac{R_s}{R_s + R_t}}} \tag{15.32}$$

The Thévenin output resistance r_t for the Op Amp alone, without feedback is typically of the order of 1000 ohms, so for large A and reasonable R_s and R_f , the overall Thévenin output resistance R_o for this topology circuit is a fraction of an ohm.

Equation 15.31 is in fact a general result. For any linear circuit in which the feed-back resistor is sampling the output *node voltage* (rather than the output current), the Thévenin equivalent output resistance with feedback is equal to the output resistance without feedback, divided by a factor 1+ (loop gain), the same factor involved in gain calculations and calculation of sensitivity to changes in the gain constant A.

15.4.2 Input Resistance, Inverting Connection

To calculate the Thévenin-equivalent input resistance of the inverting Op Amp circuit, we apply a test source at the input, and measure the resulting response. (There are no internal independent sources to be set to zero.) In Figure 15.12 we have chosen to drive with a test voltage v_t , and calculate the resulting current i_t . As before, it is equally valid to apply a test current source, and calculate the resulting voltage. The calculations are greatly simplified if the circuit topology is taken into account. The input consists of two elements in series: the resistor R_s , and a complicated circuit which will reduce to the Thévenin-equivalent input resistance of the rest of the Op Amp circuit. Recognizing this, we can first calculate the resistance to the right of the R_s (just set R_s to zero in Figure 15.12) and then add R_s to this calculated value to get the complete answer. We will denote the resistance of the Op Amp circuit to the right of R_s as R_i , and the complete input resistance, including resistor R_s , as R_i' .

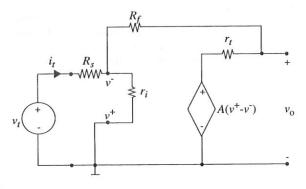


Figure 15.12: Input resistance calculation

Because we chose a test voltage, and R_s is zero for now, the control variable is directly constrained:

$$v^+ = 0 (15.33)$$

$$v^- = v_t \tag{15.34}$$

Now apply KCL at the input node

$$i_t = \frac{v_t}{r_i} + \frac{v_t - A(v^+ - v^-)}{R_t + r_t}$$
 (15.35)

Whence

$$\frac{i_t}{v_t} = G_i = \frac{1}{r_i} + \frac{1}{R_f + r_t} + \frac{A}{R_f + r_t}$$
 (15.36)

Again we have the sum of three conductances. So the corresponding resistance expression, the Thévenin input resistance for the circuit, is the parallel combination of three terms:

$$R_i = r_i \| (R_f + r_t) \| \left(\frac{R_f + r_t}{A} \right)$$
 (15.37)

the Op Amp input resistance, the feedback resistor plus Op Amp output resistor, and an effective resistance generated by the feedback. For large A,

$$R_i \simeq \frac{R_f + r_t}{A} \tag{15.38}$$

that is, we expect the input resistance to be *very low*. For example, for a typical case of $R_f = 10k\Omega$, $r_f = 1000$ ohms, $A = 10^5$, the input resistance measured at the v^- terminal

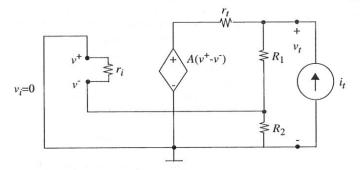


Figure 15.13: Output resistance calculation, non-inverting circuit

will be 0.1 ohm. Simple physical reasoning serves to support this result. If we imagine applying a small voltage to the input, say 0.1 mV, then the Op Amp will immediately drive v_0 to -A times 0.1 mV, or -10 volts. So resistor R_t has a large voltage across it, hence a large current will flow. This large current must come from the input source, and is 105 times as large as one might expect for such a small input voltage. Large current for small voltage means the effective input resistance will be very small, in fact roughly the feedback resistor R_f divided by A.

In accordance with our initial assumptions, the complete input resistance of the inverting Op Amp, including resistor R_s , is

$$R_i' = R_i + R_s {15.39}$$

as can be verified by calculating the input resistance directly from Figure 15.12 including R_s . Because R_i is so small,

$$R_i' \simeq R_s \tag{15.40}$$

Input and Output R for Non-Inverting Op Amp

The active-region output resistance of the non-inverting Op Amp circuit can be calculated in much the same way as for the inverting circuit. We set the independent source to zero and apply a test current source to the output terminals, as shown in Figure 15.13. Now calculate v_t . As usual, we apply the node method to find three independent equations. First find expressions for v^+ and v^- , and then write KCL at the output node. Again we assume r_i is much larger than R_2 to simplify the math.

$$v^+ = 0 (15.41)$$

$$v^{-} = v_t \frac{R_2}{R_1 + R_2} \tag{15.42}$$

$$i_t - \frac{v_t}{R_1 + R_2} - \frac{v_t - A(v^+ - v^-)}{r_t} = 0 ag{15.43}$$

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Hence

$$\frac{i_t}{v_t} = G_o = \frac{1}{R_1 + R_2} + \frac{1}{r_t} + \frac{AR_2/(R_1 + R_2)}{r_t}$$
(15.44)

For large A and reasonable R_1 and R_2 ,

$$R_o \simeq \frac{r_t}{AR_2/(R_1 + R_2)}$$
 (15.45)

This is the Thévenin output resistance r_t of the Op Amp alone, divided by the loop gain, or, more accurately, from Equation 15.44, 1 + (loop gain). As before, the output resistance is very low.

The input resistance for the active (nonsaturated) region can be found from the circuit in Figure 15.14. As before, we need expressions for v^+ and v^- , and a KCL equation involving i_t .

$$v^+ = v_t \tag{15.46}$$

$$v^- = v_t - i_t r_i \tag{15.47}$$

KCL at Node 1 yields

$$i_t + \frac{A(v^+ - v^-) - v^-}{R_1 + r_t} - \frac{v^-}{R_2} = 0$$
 (15.48)

Substituting and solving, assuming A is large, we find

$$R_i = \frac{v_t}{i_t} \simeq r_i \left[\frac{AR_2}{R_1 + r_t + R_2} \right]$$
 (15.49)

This expression shows that for the non-inverting connection, the effective input resistance in the active region is very high, (roughly the Op Amp input resistance r_i multiplied by the loop gain) in contrast to the result for the inverting case, Equation 15.38. Reasoning physically, if we apply a voltage v_t at the input, the output voltage adjusts itself so that v^- is very nearly equal to v_t , so there is very little voltage across r_i , hence much less current flowing in it than we might expect. Hence the circuit input resistance

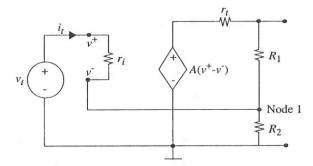


Figure 15.14: Input resistance calculation, non-inverting Op Amp

is large. This property enables the non-inverting connection to be particularly useful in buffering applications.

This point of view suggests an alternative approach to the calculation. If we assume at the outset that $v^+ - v^- \simeq 0$, then

$$v_t \simeq A(v^+ - v^-) \frac{R_2}{R_2 + R_1 + r_t}$$
 (15.50)

But $v^+ - v^-$, although small, must not be zero for finite r_t :

$$v^+ - v^- = i_t r_t \tag{15.51}$$

When Equation 15.51 is substituted into Equation 15.50, we find R_i as before (Equation 15.49).

15.4.4 Generalization on Input Resistance *

It is obviously of some importance to the circuit designer to know whether feedback is going to increase or decrease the effective input resistance of a circuit. We can generalize from the two circuits we have examined to state that the effect of feedback on input resistance depends on the *circuit topology*. If the source current and the current through the feedback resistor and the current through the Op Amp input resistor r_i all sum at a common *node* as in Figure 15.12, then the effective input resistance is very *low*, as shown in Equations 15.36 and 15.38. (Remember, here we are referring to R_i , the resistance of the Op Amp circuit to the right of R_s .) Equation 15.36 is in fact a general result: the input conductance for any feedback circuit with this input topology

(neglecting r_i) is the conductance without feedback, here $1/(R_f + r_t)$, multiplied by 1 + A.

If on the other hand, the source and the Op Amp input resistor are in series, forming a *loop* with the feedback resistor, as in Figure 15.14, the effective input resistance of the circuit will be very *high*. In a word, if at the Op Amp input we *sum currents* at a node, the circuit input resistance is *low*, if we *sum voltages in a loop*, the input resistance is *high*.

15.4.5 Example: Op Amp Current Source

We have shown that both the inverting and non-inverting Op Amp connections have very low output resistance, that is, they approximate ideal voltage sources. But in some circuit applications, we may want the Op Amp to look like a current source, that is, we want a very *high* output resistance. It follows from the discussion at the end of Section 15.4.1 that such a design can be realized by a change in the *topology of the output circuit*.

In the two circuits already discussed, the feedback network sends a signal back to the negative input terminal that is proportional to the *output voltage* v_o . Thus the circuit tends to stabilize this variable, thereby creating a voltage source. By analogy, to make a current source, we must arrange to feed back a signal proportional to the *output current* flowing in the circuit being driven by the Op Amp. One possible topology is shown in Figure 15.15a. The circuit looks, at first glance, like the non-inverting connection shown in Figure 15.15b, but there is an important difference. In the new topology, the resistor R_L we are trying to drive is now part of the voltage divider feedback network. Thus in Figure 15.15a we are using the resistor R_s to sample the current through R_L , whereas in (b) R_1 and R_2 sample the voltage across R_L . The distinction seems trivial until we think in terms of R_L varying in value, or even being nonlinear. Then it is clear that there is a fundamental difference in the two topologies.

Once the topological issues are understood, the circuit analysis is trivial. Assuming $v^+\simeq v^-$, we note from Figure 15.15a or c

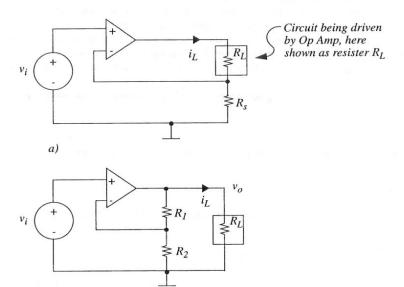
$$v^+ = v_i \tag{15.52}$$

$$v^- = i_L R_s \tag{15.53}$$

$$v^+ \simeq v^- \tag{15.54}$$

Therefore

$$i_L \simeq \frac{v_i}{R_s} \tag{15.55}$$



b) Standard non-inverting connection

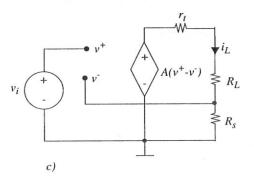


Figure 15.15: Op Amp current source

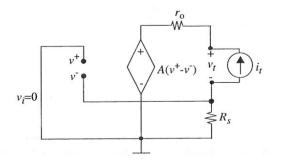


Figure 15.16: Output resistance of current source

independent of the value of R_L .

The fact that the current through R_L is independent of the value of R_L suggests that the Op Amp circuit looks like a current source. It is a simple matter to verify this more formally: replace R_L by a test source, and find the Thévenin output resistance of the circuit. In this case we choose a test current source i_t , as in Figure 15.16.

$$v^- = -i_t R_s \tag{15.56}$$

$$v^+ = 0 (15.57)$$

$$v_t = A(v^+ - v^-) + i_t r_o - v^- (15.58)$$

$$= (1+A)i_t R_s + i_t r_o (15.59)$$

$$R_o = \frac{v_t}{i_t} = (1+A)R_s + r_o (15.60)$$

For reasonable circuit parameters, R_o could well be many megohms.

Again these results can be generalized to summarize the effect of negative feedback on the effective output resistance of a circuit. If the Op Amp, the load resistor R_L and the feedback network appear to be connected in series, in a loop, hence sharing a common current, then the output resistance will be high. If the Op Amp, R_L , and the feedback circuit all appear to be in parallel, tied to a common node, sharing a common voltage, then the output resistance will be low.

15.5 Additional Examples

This section contains a number of examples of Op Amp circuits. They are intended both to illustrate the versatility of the Op Amp as a circuit design building block and

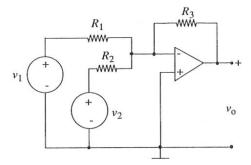


Figure 15.17: Adder

to serve as a review and extension of analysis techniques introduced earlier in this chapter.

15.5.1 Adder

An Op Amp circuit for adding two signals together is shown in Figure 15.17. If we assume $v^+ \simeq v^-$, then application of KCL to the v^- node yields

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_o}{R_3} \simeq 0 \tag{15.61}$$

Therefore

$$v_o \simeq -\left(\frac{R_3}{R_1}v_1 + \frac{R_3}{R_2}v_2\right) \tag{15.62}$$

which represents the weighted sum of the two input signals.³ Note that within the accuracy of the voltage constraint $v^+ - v^- \simeq 0$, the two input signals do not cross-couple, that is, no current from v_2 flows in R_1 , and vice versa. Thus the circuit is an *ideal adder*.

15.5.2 Subtracter

If we wish to take the difference between two signals, then the circuit of Figure 15.18 is appropriate. Direct application of superposition to the *independent sources* yields

the two subcircuits shown in Figure 15.18b and c. In (b), source v_2 has been set to zero. On the assumption of $i^+ \simeq 0$, there will be no current through R_3 and R_4 , so $v^+ \simeq 0$, and the topology is seen to be that of an inverting amplifier. Hence

$$v_{oa} = -\frac{R_2}{R_1} v_1 \tag{15.63}$$

When source v_1 is set to zero, and the circuit slightly rearranged, the non-inverting topology emerges, with a voltage divider at the input, as indicated in Figure 15.18c. Hence

$$v_{ob} = \left(\frac{R_1 + R_2}{R_1}\right) \left(\frac{R_4}{R_3 + R_4}\right) v_2 \tag{15.64}$$

The total output voltage is the sum of the two voltages v_{oa} and v_{ob} . To make a subtracter, the resistor ratios in Equations 15.63 and 15.64 should be equal. This can be achieved by setting $R_3 = R_1$ and $R_4 = R_2$. Then

$$v_o = \frac{R_2}{R_1} (v_2 - v_1) \tag{15.65}$$

Now v_o is proportional to the difference between the two input voltages.

15.6 Op Amp RC Circuits

15.6.1 Op Amp Integrator

The circuit in Figure 15.19 gives a much closer approximation to ideal integration than the simple RC circuits discussed in Chapter 10. The analysis to show this is quite straightforward. Assuming linear-region operation, we replace the Op Amp by the dependent-source model, as in Figure 15.19b, and analyze the resulting linear circuit using the node method. KCL at the v^- node yields

$$\frac{v_i - v^-}{R} + \frac{Cd(v_o - v^-)}{dt} = 0 {(15.66)}$$

If we assume at the outset that the Op Amp gain A is large enough to ensure that

$$v^+ \simeq v^- \tag{15.67}$$

then because $v^+ = 0$, Equation 15.66 reduces to

³Because the Op Amp model is linear, the same result can be derived using superposition as well.

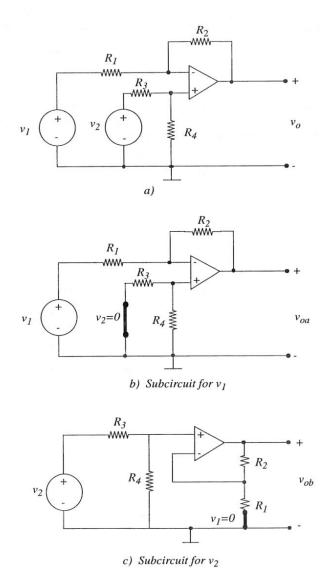
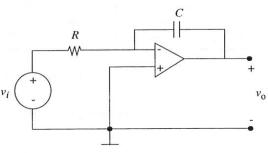
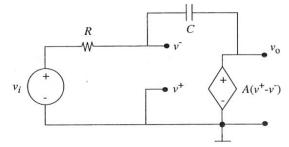


Figure 15.18: Subtracter



a) Circuit



b) Active region subcircuit

Figure 15.19: Op Amp Integrator

$$\frac{v_i}{R} + \frac{Cdv_o}{dt} \simeq 0 \tag{15.68}$$

or,

$$v_o \simeq -\frac{1}{RC} \int v_i dt \tag{15.69}$$

That is, the circuit calculates the (negative) integral of the input voltage.

A more exact calculation involves substituting the Op Amp equation

$$v_o = A(v^+ - v^-) (15.70)$$

into Equation 15.66, again noting $v^+ = 0$

$$\frac{v_i}{R} - \frac{v_-^-}{R} - CA\frac{dv_-^-}{dt} - C\frac{dv_-^-}{dt} = 0$$
 (15.71)

Hence

$$RC(1+A)\frac{dv^{-}}{dt} + v^{-} = v_{i}$$
 (15.72)

The effective time constant of the circuit (by analogy with Equation 10.150, for example) is

$$\tau = (1+A)RC\tag{15.73}$$

Thus the time constant associated with the passive elements alone is multiplied by the gain of the Op Amp. This is often referred to as the Miller Effect, originally in reference to the fact that a small input to output capacitance in early vacuum tubes seriously limited the frequency response of amplifier circuits. The time constant can be made very large for modest component values. For example, if the RC time constant is 1 second, and A is 10⁵ or greater, the effective circuit time constant in measured in days. On this time scale almost any waveform lasting for less than a minute or so will seem like a "short pulse". Thus the analysis of Section 10.6.3 is applicable, and on the time scale of minutes, the circuit acts like an Integrator.

The ultimate test of an Integrator is to apply a small voltage step, V, and see how closely the Integrator output conforms to a ramp. From Equations 15.70 and 15.72,

$$(1+A)RC\frac{dv_o}{dt} + v_o = -AV (15.74)$$

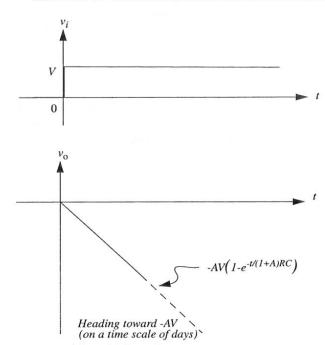


Figure 15.20: Waveforms of integrator

For v_i a small fixed value V after t=0, v_o will follow the usual exponential charging curve toward (-AV), (see Equation 10.101, for example). That is,

$$v_o = -AV \left(1 - e^{-t/(1+A)RC} \right) \tag{15.75}$$

This curve is plotted in Figure 15.20 on the basis that the RC time constant (without the Op Amp) is roughly one second. Obviously on the time scale of minutes, the circuit looks like an almost-perfect integrator, provided, of course, the Op Amp is always operating in the active region.

15.6.2 Op Amp Differentiator

The Op Amp differentiator shown in Figure 15.21 complements the integrator. Because $v^- \simeq v^+$ and $v^+ = 0$, we know that the current i_1 through the capacitor is given

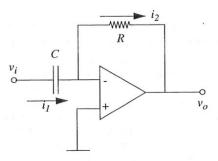


Figure 15.21: Differentiator circuit

by

$$i_1 = C \frac{dv_i}{dt}$$

Since virtually no current flows into the Op Amp, $i_1 = i_2$, and therefore

$$v_o = -Ri_1$$

Eliminating i_1 from the above two equations, we obtain

$$v_o = -RC\frac{dv_i}{dt} \tag{15.76}$$

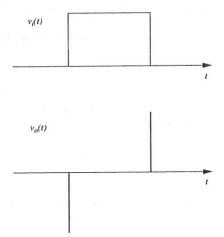
That is, this circuit calculates the (negative) time derivative of the input voltage.

Sample input and output waveforms for the differentiator are shown in Figure 15.22. For the square pulse input shown, the outputs are a pair of spikes each at the time instant the input makes a transition. As illustrated in the example, the differentiator circuit is often used in detecting shape transitions in waveforms.

15.6.3 An RC Active Filter

An Op Amp embedded in a more complicated RC circuit is shown in Figure 15.23a. This is an RC active filter, with all of the useful resonance properties of a capacitor-inductor circuit. To show this, we calculate the output voltage v_o in terms of v_i . First draw the linear-region circuit model with the dependent source, Figure 15.23b. Then write Node equations, taking current entering the node as positive. We assume at the outset $v^+ - v^- \simeq 0$. because v^+ is zero in this circuit, the appropriate constraint is $v^- \simeq 0$. For Node v_1 ,

$$(v_i - v_1)g_1 - C_1 \frac{dv_1}{dt} + C_2 \frac{d(v_0 - v_1)}{dt} = 0$$
 (15.77)



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Figure 15.22: Differentiator waveforms

and for Node v^-

$$C_1 \frac{dv_1}{dt} + v_o g_2 = 0 (15.78)$$

Hence

$$v_i g_1 = g_1 v_1 + (C_1 + C_2) \frac{dv_1}{dt} - C_2 \frac{dv_0}{dt}$$
 (15.79)

$$0 = C_1 \frac{dv_1}{dt} + v_0 g_2 (15.80)$$

These equations can be solved by taking the derivative of both sides of both equations, and eliminating terms in v_1 and its derivative by substitution from Equation 15.80 and the derivative of Equation 15.80. By so doing we obtain a second order differential equation for v_0 :

$$\frac{d^2v_o}{dt^2} + g_2 \frac{C_1 + C_2}{C_1 C_2} \frac{dv_o}{dt} + \frac{g_1 g_2}{C_1 C_2} v_o = -\frac{g_1}{C_2} \frac{dv_i}{dt}$$
(15.81)

This equation is identical in form to that of an RLC resonator (see Equation 12.119), but this circuit contains no inductors. The effect of an inductor is created by an active element, in this case the Op Amp, and the capacitors, hence the name

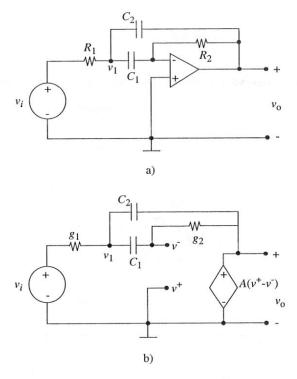


Figure 15.23: Op Amp RC active filter

RC active filter. The advantages of an RC active filter (this is only one realization; there are many others) are that it can provide a power gain unlike an RLC network and that it does not require inductors. Because inductors are difficult to fabricate in VLSI technology, this is an important design advantage for integrated circuits. Furthermore, inductors are not very ideal elements, especially for low-frequency applications (for example, for frequencies below perhaps 100 kHz). Thus in this frequency range, resonant circuits are often built out of Op Amps, resistors, and capacitors.

The properties of filter circuits were explored previously in Chapters 10 and 13. As we did in Chapter 13, the circuit of Figure 15.23 can also be analyzed using the impedance method by using impedance values $1/sC_1$ and $1/sC_2$ for the capacitors (see Section 15.6.4). We will also see other examples of impedance based analysis for Op Amps later in this chapter.

Since Equation 15.81 is identical in form to Equation 12.119 for the RLC circuit, we can readily determine the behavior of our RC active filter. Notice that the output response v_o of the Op Amp RC active filter corresponds to the capacitor voltage v_C in Section 12.5. The equation corresponding to the series RLC circuit in Section 12.5 was

$$\frac{d^2 v_C}{dt^2} + \frac{R}{L} \frac{dv_C}{dt} + \frac{1}{LC} v_C = \frac{1}{LC} v_{IN}$$
 (15.82)

with the damping factor $\alpha = \frac{R}{2L}$ and the undamped resonant frequency $\omega_o = \frac{1}{\sqrt{LC}}$.

Thus, the corresponding damping factor in our Op Amp circuit is

$$\alpha = g_2 \frac{C_1 + C_2}{2C_1 C_2} \tag{15.83}$$

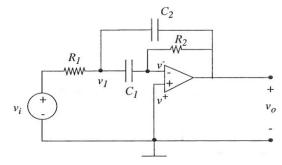
and the undamped resonant frequency is

$$\omega_o = \sqrt{\frac{g_1 g_2}{C_1 C_2}} \tag{15.84}$$

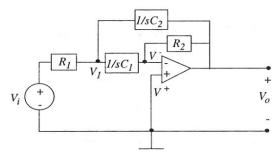
15.6.4 The RC Active Filter – Impedance Analysis

Let us analyze the Op Amp active filter circuit of Section 15.6.3 for a sinusoidal drive. Since the Op Amp is a linear device (namely, a VCVS) we can use the impedance method for the analysis.

The circuit configuration is repeated in Figure 15.24a. The impedance model for the circuit is shown in Figure 15.24b. The circuit is sufficiently complicated that node analysis is advisable. At node V_1 assuming $v^+ \simeq v^-$,



a) Circuit



b) Impedance model

Figure 15.24: RC active filter analysis using the impedance method

$$(V_i - V_1) g_1 + (V_o - V_1) sC_2 - V_1 sC_1 = 0$$
(15.85)

where $g_1 = 1/R_1$. At the V^- node,

$$V_1 s C_1 + V_0 g_2 = 0 (15.86)$$

where $q_2 = 1/R_2$.

Now V_0 can be found by Cramer's Rule. First, rewrite with source terms on the left

$$V_i g_1 = V_1 [g_1 + s (C_1 + C_2)] - V_o s C_2$$
 (15.87)

$$0 = V_1 s C_1 + V_0 q_2 (15.88)$$

(These equations should be compared to the corresponding differential equations, Equations 15.79 and 15.80). Solving for the complex amplitude V_0 ,

$$V_o = \frac{-g_1 s C_1 V_i}{[g_1 + s (C_1 + C_2)] g_2 + s^2 C_1 C_2}$$

$$= \frac{-g_1 s C_1 V_i}{g_1 g_2 + s (C_1 + C_2) g_2 + s^2 C_1 C_2}$$
(15.89)

$$= \frac{-g_1 s C_1 V_i}{g_1 g_2 + s (C_1 + C_2) g_2 + s^2 C_1 C_2}$$
 (15.90)

$$= \frac{-s\left(g_1/C_2\right)V_i}{s^2 + s\frac{C_1+C_2}{C_1C_2}g_2 + \frac{g_1g_2}{C_1C_2}}$$
(15.91)

Equation 15.91 has exactly the form of Equation 14.19 (except for the minus sign), hence the circuit is equivalent to a parallel RLC filter. By comparing corresponding terms we find, as in Chapter 12,

Resonant frequency =
$$\omega_o = \sqrt{\frac{g_1 g_2}{C_1 C_2}}$$
 (15.92)
Bandwidth = $g_2 \frac{C_1 + C_2}{C_1 C_2}$ (15.93)

Bandwidth =
$$g_2 \frac{C_1 + C_2}{C_1 C_2}$$
 (15.93)

With these scaling factors, the frequency response plot of Figure 14.12 directly applies to this circuit (except for the additional 180° in the phase), along with all other properties discussed in Section 14.1.

15.6.5 Sallen-Key Filter

This section introduces a lowpass filter called the Sallen-Key filter. Its circuit and impedance model are shown in Figure 15.25.

Let us focus on sinusoidal inputs and use the impedance method to obtain its inputoutput relationship. First, notice that the portion of the circuit within the dashed box is a non-inverting connection of the Op Amp with gain

$$G = 1 + \frac{R_1}{R_2} \tag{15.94}$$

Thus, for the purpose of analysis, we can replace the circuit within the dashed box with an amplifier whose gain is G. Therefore, we can write

$$V_o = GV_1 \tag{15.95}$$