A Change in Methodology Accelerates the Isolation in Root Cause of Defects for Improving Yield and Lowering Costs

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Abstract
This paper describes a real case where employing a change in methodology enabled the root cause of the defect to be located and confirmed in a device. Traditional methods of systematic search techniques using FA equipment, which requires weeks of effort, would not have been able to locate this defect. Layer by layer de-processing and inspection would have taken months to complete. The new methodology of performing a diagnosis on the scan failures to directly target FA experiments enabled the engineers to complete the analysis in two days.

1. Introduction
Traditionally many techniques have been deployed to locate physical defects in digital integrated circuits. These include static observation techniques such as emissions microscopy and static bias laser stimulation techniques such as Optical Beam Induced Resistance Change (OBIRCH), Voltage Bias voltage sensing Amplifier (VBA), and Thermally Induced Voltage Alteration (TIVA) [1,2,3,4,5,6]. Recently dynamic bias techniques such as Laser Assisted Device Alteration (LADA), Resistive Interconnect Isolation (RIL), and Soft Defect Localization have been used to isolate timing sensitive defects [8,9,10].

Each of these techniques requires that the device be placed into a condition that justifies the defect on the device and the effects of the defect to be observed. This poses a significant challenge to the failure analysis engineer to provide the proper conditions to justify the defect prior to performing lengthy experiments to observe the results. Many engineers will employ simple patterns and observe the device on one cycle. If this cycle fails to produce useful results, they will apply another clock cycle and start again. More advanced labs will employ Automated Test Equipment (ATE) and run the device until the cycle in which a failure is observed to begin the Failure Analysis (FA) experiments.

Scan and Automatic Test Pattern Generation (ATPG) are widely used techniques for testing digital logic on an integrated circuit. This is a very effective method for producing high quality tests with minimal development effort, but can create difficulties in determining the source of the failures. Since the failing bits are shifted out of the device for observation after the test is applied, performing FA experiments on the failing cycles is not likely to stimulate the defect for observation.

Another problem with traditional biasing techniques is that the observed results are not tightly correlated to the stimulus applied. There are many conditions, such as bus conflicts, that can result in photon emissions without a defect being present in the silicon.

This paper will present a process to significantly reduce the time required for defect isolation by using scan to accurately justify the defect, diagnose the failure data to determine the most likely place for the defect to occur, analyze the physical design to pinpoint the most likely location for the defect to be observed, and guide physical failure analysis experiments.

2. Accelerating Defect Isolation
2.1 Change of Thinking, Change of Flow
Finding physical defects in devices is historically hampered by the traditional methodology illustrated in Figure 1. In this process, the design information of the device is inaccessible to several of the engineering disciplines. By the time the failing devices are analyzed, it is difficult to determine the meaning of the collected failures. Scan and ATPG test methods can make it very difficult for a failure analysis engineer to isolate a defect location based on an understanding of the failing pins. This leads them to resort to functional testing, which does not provide sufficient information to analyze defects deep in logic of the device.
A proven methodology to better integrate the design, manufacturing, test, and failure analysis domains is presented in Figure 2. In this flow, a DFT-Enabled Engineering Test System, a Teseda V520 or V550, is used to rerun the Standard Test Interfaced Language (STIL) scan based test patterns to capture all the failures of the device as was seen in production by ATE, but with the major advantage of having significant failure capture depth. Several failing devices are tested without impacting the manufacturing flow. Large amounts of failure information can be captured from a scan test to gain a detailed understanding of the failure, even if the failure occurs in the scan chain. Teseda WorkBench (TWB) debug software is used to analyze the mismatching scan test results and isolate the failing scan chains and scan cells of the device. The system operates on STIL patterns generated by the major Design for Test (DFT) Electronic Design Automation (EDA) companies providing an interoperable workflow for devices that use any combination of vendors for scan and ATPG.

2.2 Required data
The key in this new methodology is the management of design and test data. The diagnostic tool of this flow, the Teseda Diagnostic Manager NetXY software, manages data that includes information of the physical design layout, logical design, scan definition, and test failure results. The design layout provides the physical description with XY coordinates of cells, nets, vias, and metal layers of the device under test. The logical design information provides a way to correlate the named features, such as scan cells, to the physical features of the design. The scan definition is taken from STIL that is used to provide stimulus and response data for the ATE; it provides the logical names of the scan cells and the order in which they are organized into scan chains [14].

2.2 Benefits of the new flow
With this data preserved and made available to the failure analysis team, they are able to collect large amounts of failure data for each device and use software to determine the most likely locations in the physical design for the defect to have occurred, resulting in the observed pattern of failing bits.

With specific design features identified, the FA team can perform targeted experiments to confirm their presence. This changes the process from being like finding a proverbial “needle in a haystack” to being like finding a needle in a handful of twigs. Exhaustive scanning of the device to isolate potential locations is no longer required to isolate the defect. This can remove several weeks or months from the defect isolation process, allowing the corrective action to be performed much sooner.

3. A Methodology Flow Case Study

The flow described in the previous section was used to analyze Maxim Integrated Product’s high volume commercial MAX9526 device, which is a low-power video decoder that converts NTSC or PAL composite video signals to 8-bit or 10-bit YCbCr component video compliant with the ITUR BT.656 standard.

3.1 Objective

The objective was to prove that failure analysis of devices failing the scan test could be completed to defect confirmation in less than two weeks, proving the effectiveness of the new flow described in section two.

3.2 Sample Selection

The production test team delivered a device that was failing the scan test. The test was rerun on the engineering test system to verify the correlation of the failures as seen in production. A defect-free device was also provided to verify the test fixture and test setup. As there was only one defective sample to work with, it was critically important to identify the defect location prior to performing destructive analysis.

3.3 Identify failures in logical design

The DFT-Engineering test system with scan debug software was used as depicted in Figure 2. The device was configured with socket and board to interface with the test system. The STIL patterns were then run on the device with the test system. The failure results of the scan tests were captured in failure logs that reported the cycle in which the mismatch of the expected result occurred, the scan chain number, and the index of the scan cell reporting the mismatch. Within the system debug software, details of mismatching scan cells in the logical hierarchy of the design and scan chain within the design blocks were analyzed.

Four scan cells were found to be failing frequently, with a few infrequent failures on surrounding scan cells. All of these scan cells were located in the same logic block of the design.

3.4 Employing Traditional FA with defect targeted stimulus

The next step was an attempt to use the engineering test system to provide accurate stimulus to justify the defect and perform emissions microscopy and XIVA experiments.

The device was de-capsulated on the topside for these experiments; the fixture that was used did not allow for backside experiments. Taking advantage of its small footprint and pattern execution control, the engineering test system placed inside the microscopy chamber, Figure 3, and the device was run to the point in the pattern where the defect was justified. As this was a scan test, this was a simple matter of inserting a pause at the beginning of the capture cycle before the mismatches occurred.

Despite use of this equipment and set up, it proved inconclusive and was not able to determine the location of the defect. The effectiveness of the emissions microscopy test was diminished due to the inability to view the backside of the die during the
test. XIVA can be effective by heating the defective net. As will be shown later, the defect was on a lower layer making it more difficult to obtain a reliable result.

3.5 Using software to isolate the defect

Using the Teseda Diagnostic Manager software as shown in Figure 2, the design was analyzed by tracing the inputs of the failing scan cells to a point where the paths converged.

As mentioned earlier, four key scan cells were identified as reporting the most significant number of mismatches during the scan test. The location, XY coordinates, of these scan cells were highlighted against the physical layout of the design. By tracing the D-inputs of these scan cells, it was discovered that the scan cells shared the common net shown in Figure 4. This type of net convergence poses the high likelihood that the defect is located on this net or the gate that drives it.

From here the net was analyzed to find design features, such as stacked vias, that are more prone to failure than others. With the layer viewing capabilities of the tool, the suspect net could be traced between layers of the design. By selectively turning on and off layers of interest, the location of where the net crossed from METAL2 to METAL4 with stacked single vias was analyzed (shown in Figure 5). This net crossing became the prime suspect.

3.6 Confirming the defect with Physical experiments

This device had six layers of metal and, as the only sample, it was desirable to find points on the top layer to insert micro-probe points in order to avoid unwanted damage. By tracing the net in the diagnostic software, suitable points were found on this net. Points on adjacent and nearby nets were also identified for the micro-probing experiments. A Focused Ion Beam (FIB) was used to insert the probe contact points and then traditional probing was used to perform continuity tests between these points.

The provided probe points, shown in the Figures 6 and 7, were determined by investigation of the common nets in the diagnostic software. The background in both these figures is a “zoomed in” view of the layout representation of the physical device highlighting the suspect area of the defect. The highlighted scan cells in Figure 7 are identified as reported by the failure results. The common nets of the failure results are shown running north and south in the diagnostic software. The points of interest for the FIB are selected and noted as FIB Points A through E against the background of the layout.
The continuity tests showed that there is one diode between FIB point A, and points B, C, and E. This would indicate that there is contact from each of these nets to the silicon at some point.

As shown in Figure 8, the input of the gate is connected to the gate of the transistors and the output is connected to the drain. Figure 9 illustrates that the gate of the transistors is insulated from the silicon with a dielectric layer, but the drain is connected directly to the silicon [13]. This means that only the outputs of the gates make direct contact to the silicon.

In this case, the outputs of all of the probed nets are at the north end of the net. This would indicate that there are no opens between each of these FIB points and the north end of the net. It can also be concluded that these nets are not shorted to each other.

More details of the nets of interest can be seen on the layer that best shows them without the presence of other layers obstructing the view. Figures 10 and 11 illustrate the determined FIB points with only the top metal layer visible.
FIB point B is the suspect net and it was determined that there were no opens on this net from this point to the north. It must now be determined if there is connection to the gate that is driven by this net.

To determine this, two additional FIB points were selected. FIB point X, as shown in the Figure 12, is located on the net that is on the output of an inverter, which our suspect net is driving. FIB point Y is connected to the output of a nearby inverter. The continuity test should reveal at least one diode between these points to confirm that FIB point X is connected to the output of the inverter. From here, there should be a logical inversion between FIB point B and FIB point X.

The device was then taken to the micro probing station where the continuity test confirmed the connection from FIB point X to the gate. The device was then powered-up and a signal was applied to FIB point B. No signal was observed on FIB point X, indicating that the inverter was not receiving the signal. These experimental results confirmed that the defect was located on the portion of the net that was originally identified using the diagnostic software.

There were two via locations between the probe point and the gate of the transistor that could contain the defect. Both locations were accessible with one cross-section of the device. After cross sectioning the device, SEM revealed an open defect was found on the METAL2 to METAL1 via. Figure 13 shows the diagnostic software detail view of the same location, but in higher resolution, as originally identified. The METAL1 layer is also included in this version and the image has been rotated to match the orientation of the SEM image.

4. Variations of the flow

What has been shown in this paper is an example of the flow presented in Figure 2. This process can include the incorporation of ATPG based diagnosis tools. Figure 14 gives an example of the flow that includes EDA DFT software that provides logical defect candidates, typically given in gate/cell information. These logical defect candidates are read into the Teseda diagnostic software tool where physical XY coordinates are correlated with the EDA information. These additional cell candidates are then used as part of the defect search.

In another example, the flow is adapted to having ATE as the diagnosing hardware. In Figure 15, the Teradyne J750 and UltraFlex testers provide the scan
test results to the same scan debug software used on the engineering test system [15]. The debug software performs analysis on the failure data from mismatching scan chains and respective cells. The database of the accumulated failures results of test(s) along with all associated analyzed data can be directly fed to the diagnostic management software for physical coordination and isolation of the defect in the manner as described in section 3.

5. Conclusions

The root cause of the defect was found in two days proving the new flow to be extremely effective. The resulting cost savings in time, equipment, and manpower enable this to be used on an extremely high mix of devices at Maxim Integrated Products. Traditional techniques would have taken weeks or months to complete, rendering them ineffective.

The diagnostic management software, NetXY, manages all the scan failure data from multiple scan testing experiments and analyses and then maps the physical locations of scan cells to the reported scan mismatches. It then displays the physical layout view of the device under test. Logical defect candidates are shown on the physical design with the XY coordinates of the identified features. This minimizes the physical search area required to locate defect on the device. Using a targeted search dramatically reduced the amount of time spent on the FA equipment.

Figure 14. Flow with the inclusion of EDA tools
FA equipment (emission microscope, XIVA and OBIRCH) was not able to locate this defect. Using diagnostic software to analyze the failure data and guide experiments allowed the defect to be pinpointed and confirmed by micro probing. Thus the omission of using FA equipment in this step could have further reduced the effort to find the defect down to one day instead of two.

Although the emission microscope, XIVA and OBIRCH did not prove successful, the portability of a small DFT engineering test system across these two different analysis platforms was very valuable because the device could be justified to the exact condition that stimulates the defect. This significantly reduced the amount of time required to find the failing condition. Since the same test that was used on production ATE could be run on the engineering test system with the same results correlation to the test floor is ensured. The large capture memory of the engineering test system allows enough data to be captured to effectively diagnose many types of failures.

6. References


